EUV Lithography

Introduction, Status and Challenges

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Outline

- Introduction to EUV Lithography
- Technical Status and Challenges
- Summary

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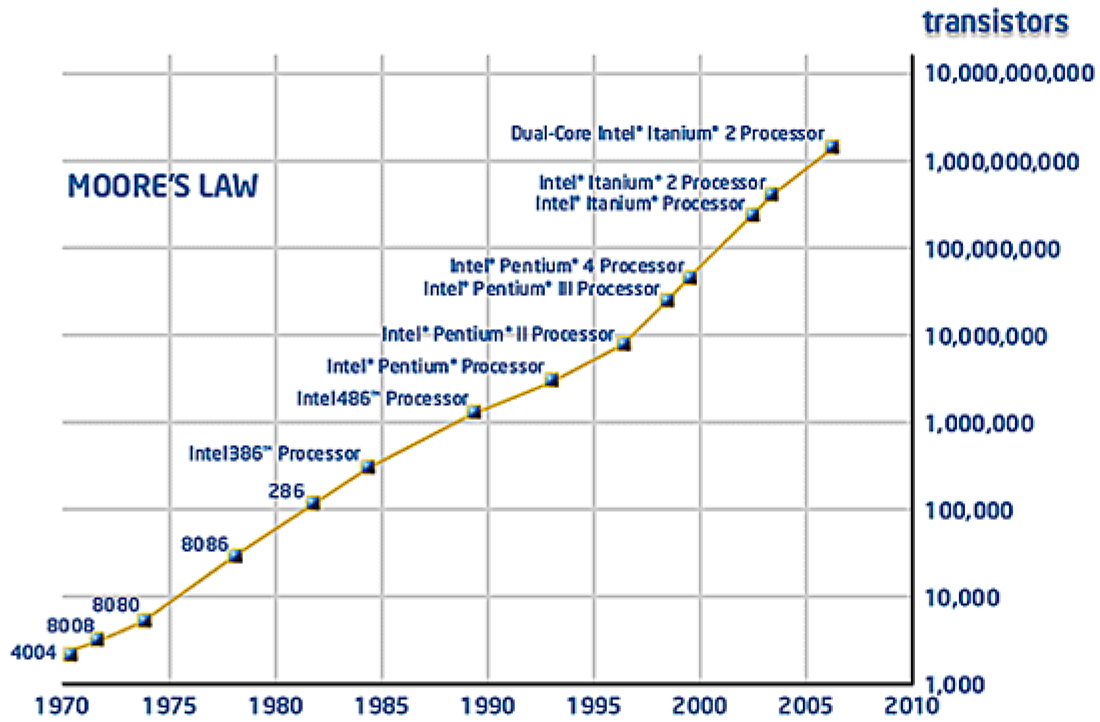
Introduction to EUV Lithography:
Moore's Law: *Number of transistors on a chip doubles about every two years.*



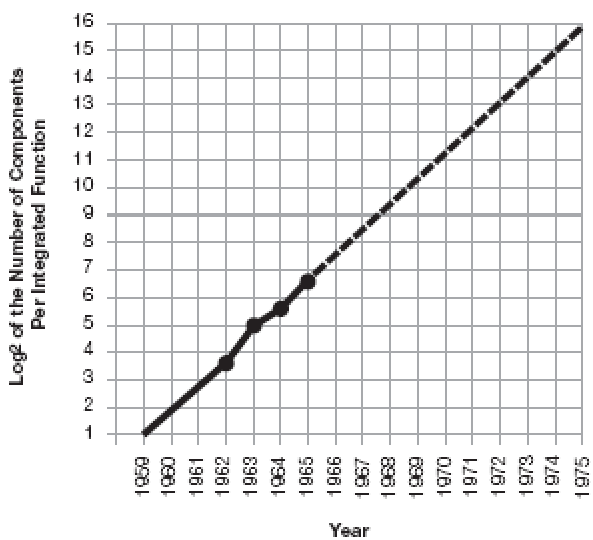
Source: http://www.intel.com/technology/mooreslaw/index.htm

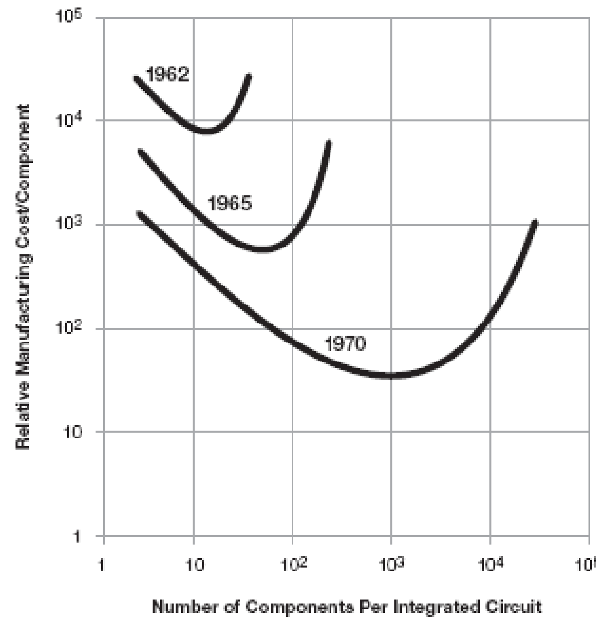
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.





Electronics, Volume 38, Number 8, April 19, 1965

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Introduction to EUV Lithography:
EUVL is the leading Lithography Technology for 22 nm node and Beyond (2009 ITRS)

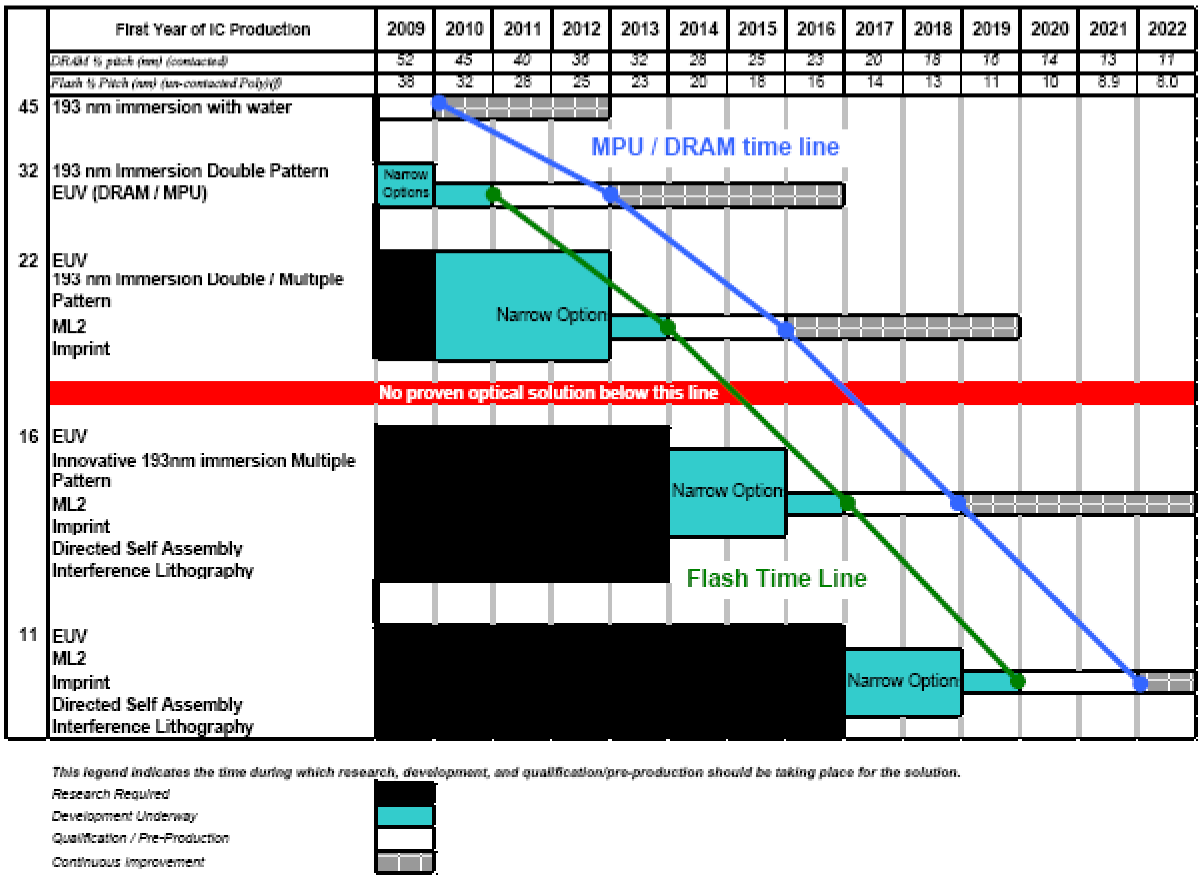


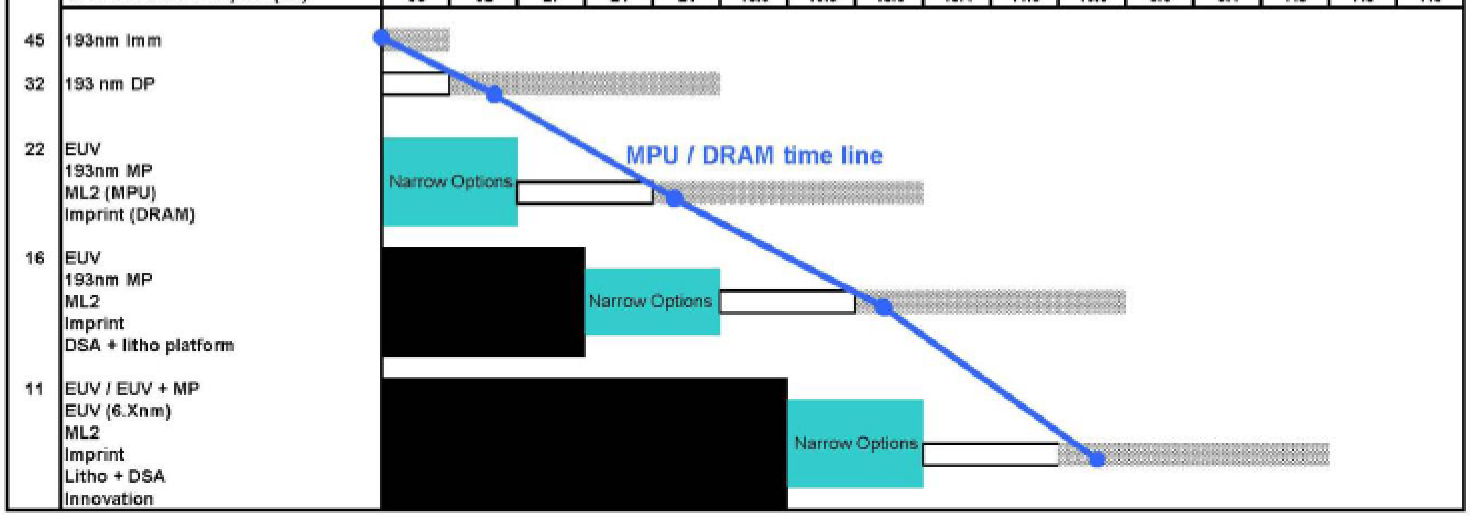
Figure LITH3 Lithography Exposure Tool Potential Solutions

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: *2009*

www.itrs.net

Introduction to EUV Lithography:
EUVL is the leading Lithography Technology for 22 nm node and Beyond (2011 ITRS)

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
MPU/ASIC Metal 1 1/2 pitch (nm)	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	7.5	7.5



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Figure LITH3A Lithography Exposure Tool Potential Solutions for MPU and DRAM Devices

EUVL Offers Cost Effective Solution to Continue Moore's Law

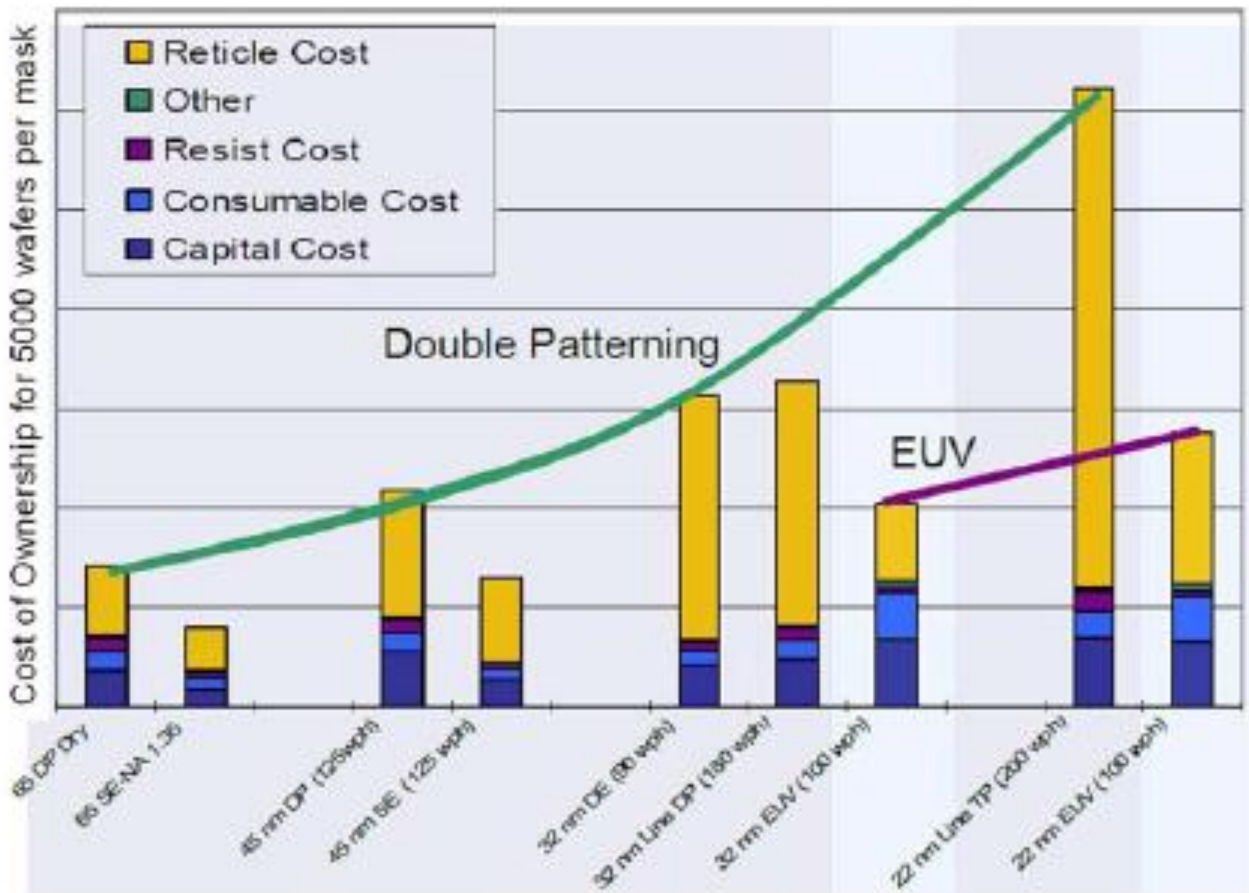
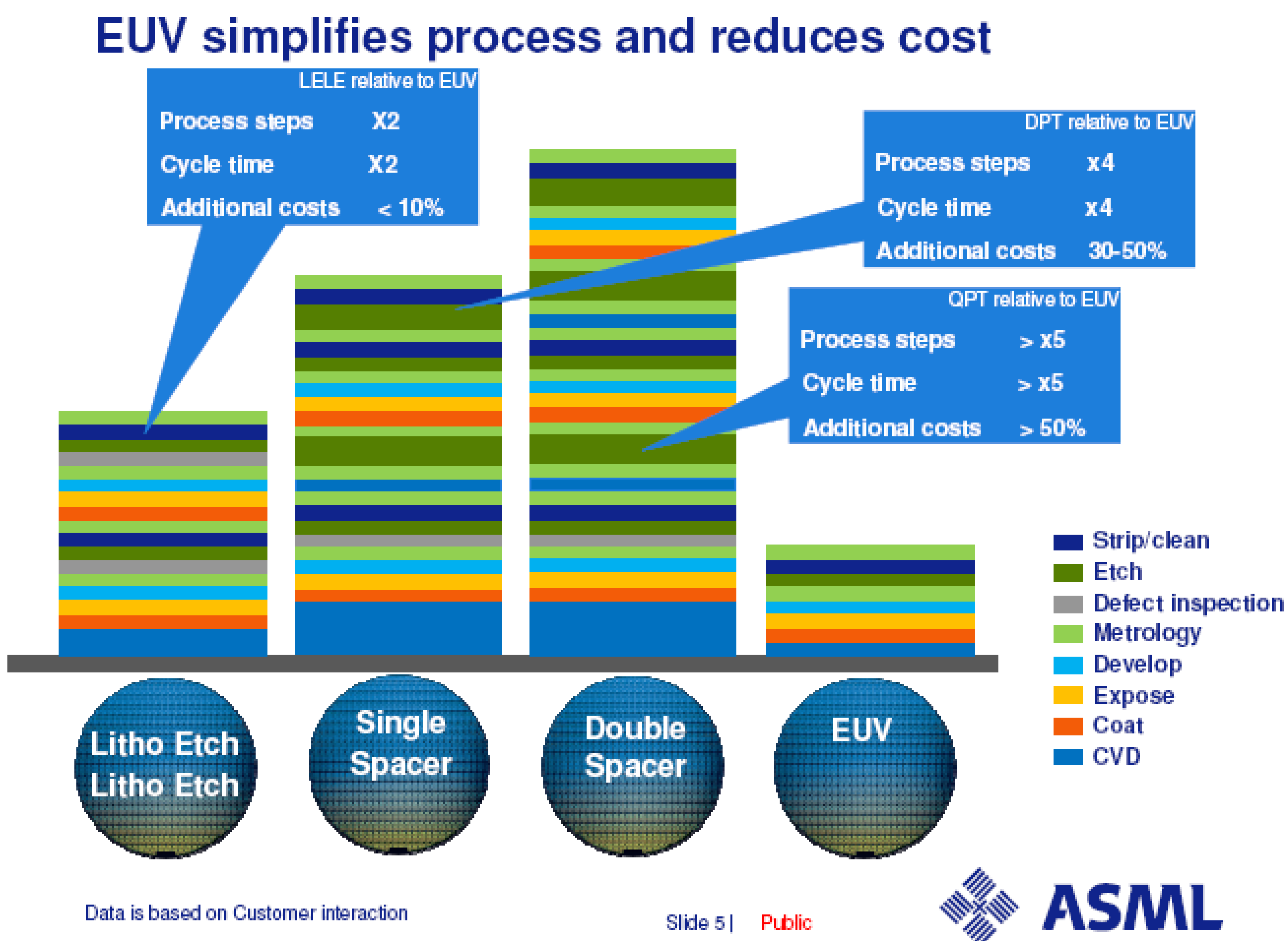


Figure LITH2 Relative Cost of Ownership for the critical level of a 5000 wafer run device

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: *2009*

EUVL Offers More Cost Effective Solution than 193 nm Double Patterning



Rudy Peeters, ASML, 2011 EUVL Symposium

Introduction to EUV Lithography:
Resolution Criterion

$$\text{Resolution} = k1 \frac{\lambda}{NA}$$

NA = numerical aperture of imaging optics * n (refractive index) * sin θ

K1	Solution
>0.55	Binary Mask + Simple Illumination
0.45 ~ 0.55	Binary +Attenuated PSM +OPC + Off-axis illumination
0.35-0.45	Alternating / Chromeless PSM +OPC + Complex Illumination + Design Restriction
0.25-0.35	Innovative Solutions
<0.25	Below Diffraction Limit

"Effective k1" can be below 0.25 by using techniques such as "Double Patterning" (via splitting of features or pattern)

Cost effectiveness and overlay are issues for this technology

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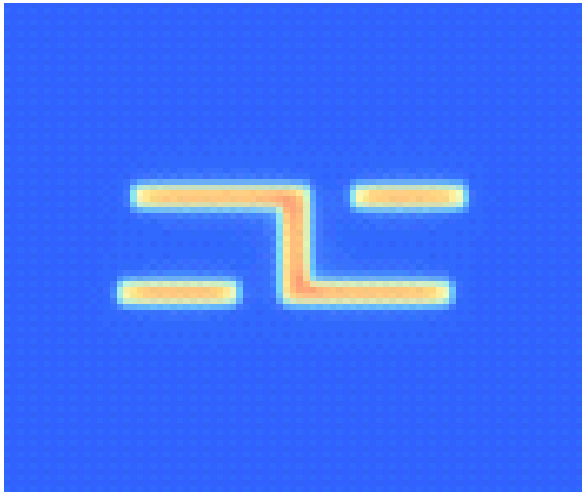
Introduction to EUV Lithography
EUVL Advantage :
k1 value vs. optical image quality

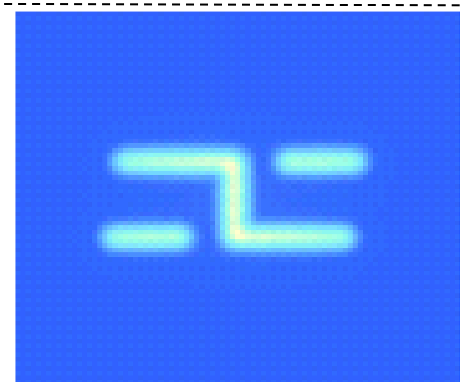


32nm hp

K1=0.59
32nm hp @EUVL NA0.25

K1=0.25
32nm hp @ArF Immersion

22nm hp



K1=0.41
22nm hp @EUVL NA 0.25

Ref: T. Miura, Nikon Corporation, 2006 International EUVL Symposium, Barcelona, Spain, October 16, 2006

Wavelength Reduction has been a key Driver of Moore’s Law

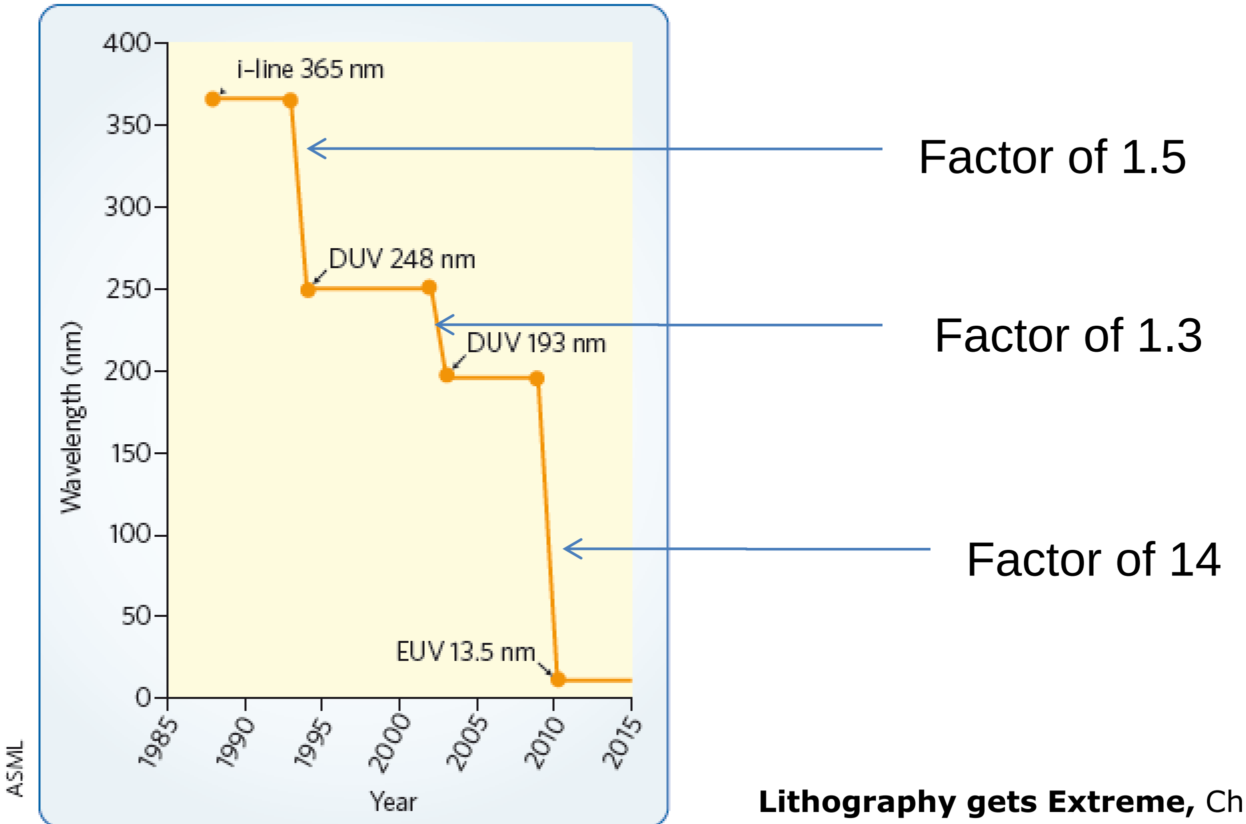


Figure 1 | Since the mid-1980s, the wavelength of light used in lithography systems has reduced by almost half from 365 nm to 193 nm. The switch to EUV lithography involves a further wavelength reduction factor of almost 15. DUV, deep ultraviolet.

Lithography gets Extreme, Christian Wagener and Noreen Harned, Nature Photonics, Vol. 4, pp. 24-26, January 2010

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Introduction to EUV Lithography:

Patterning with EUV (13.5 nm) offers higher k1 value than for 193 nm

Resolution ↓ NA →

193 nm

	0.25	0.35	0.45	0.55	0.65	0.75	0.85	0.95	1.05	1.15	1.25	1.35	1.45	1.55
90	0.12	0.16	0.21	0.26	0.30	0.35	0.40	0.44	0.49	0.54	0.58	0.63	0.68	0.72
65	0.08	0.12	0.15	0.19	0.22	0.25	0.29	0.32	0.35	0.39	0.42	0.45	0.49	0.52
45	0.06	0.08	0.10	0.13	0.15	0.17	0.20	0.22	0.24	0.27	0.29	0.31	0.34	0.36
32	0.04	0.06	0.07	0.09	0.11	0.12	0.14	0.16	0.17	0.19	0.21	0.22	0.24	0.26
22	0.03	0.04	0.05	0.06	0.07	0.09	0.10	0.11	0.12	0.13	0.14	0.15	0.17	0.18
11	0.01	0.02	0.03	0.03	0.04	0.04	0.05	0.05	0.06	0.07	0.07	0.08	0.08	0.09

13.5 nm

	0.25	0.35	0.45	0.55	0.65	0.75	0.85	0.95	1.05	1.15	1.25	1.35	1.45	1.55
90	1.67	2.33	3.00	3.67	4.33	5.00	5.67	6.33	7.00	7.67	8.33	9.00	9.67	10.33
65	1.20	1.69	2.17	2.65	3.13	3.61	4.09	4.57	5.06	5.54	6.02	6.50	6.98	7.46
45	0.83	1.17	1.50	1.83	2.17	2.50	2.83	3.17	3.50	3.83	4.17	4.50	4.83	5.17
32	0.59	0.83	1.07	1.30	1.54	1.78	2.01	2.25	2.49	2.73	2.96	3.20	3.44	3.67
22	0.41	0.57	0.73	0.90	1.06	1.22	1.39	1.55	1.71	1.87	2.04	2.20	2.36	2.53
11	0.20	0.29	0.37	0.45	0.53	0.61	0.69	0.77	0.86	0.94	1.02	1.10	1.18	1.26

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Introduction to EUV Lithography:

Patterning with Double patterning reduces k1 and further reduction of wavelength allows relaxed NA

Resolution (HP) →

NA	32	28	25	22	20	18	16	14	13	11	10	9	8
193 nm (DP)													
1.30	0.22	0.19	0.17	0.15	0.13	0.12	0.11	0.09	0.09	0.07	0.07	0.06	0.05
1.35	0.22	0.20	0.17	0.15	0.14	0.13	0.11	0.10	0.09	0.08	0.07	0.06	0.06
EUV 13.5 nm													
0.25	0.59	0.52	0.46	0.41	0.37	0.33	0.30	0.26	0.24	0.20	0.19	0.17	0.15
0.33	0.78	0.68	0.61	0.54	0.49	0.44	0.39	0.34	0.32	0.27	0.24	0.22	0.20
0.35	0.83	0.73	0.65	0.57	0.52	0.47	0.41	0.36	0.34	0.29	0.26	0.23	0.21
0.40	0.95	0.83	0.74	0.65	0.59	0.53	0.47	0.41	0.39	0.33	0.30	0.27	0.24
0.45	1.07	0.93	0.83	0.73	0.67	0.60	0.53	0.47	0.43	0.37	0.33	0.30	0.27
0.50	1.19	1.04	0.93	0.81	0.74	0.67	0.59	0.52	0.48	0.41	0.37	0.33	0.30
EUV 6.7 nm													
0.25	1.19	1.04	0.93	0.82	0.75	0.67	0.60	0.52	0.49	0.41	0.37	0.34	0.30
0.33	1.58	1.38	1.23	1.08	0.99	0.89	0.79	0.69	0.64	0.54	0.49	0.44	0.39
0.35	1.67	1.46	1.31	1.15	1.04	0.94	0.84	0.73	0.68	0.57	0.52	0.47	0.42
0.40	1.91	1.67	1.49	1.31	1.19	1.07	0.96	0.84	0.78	0.66	0.60	0.54	0.48
0.45	2.15	1.88	1.68	1.48	1.34	1.21	1.07	0.94	0.87	0.74	0.67	0.60	0.54
0.50	2.39	2.09	1.87	1.64	1.49	1.34	1.19	1.04	0.97	0.82	0.75	0.67	0.60

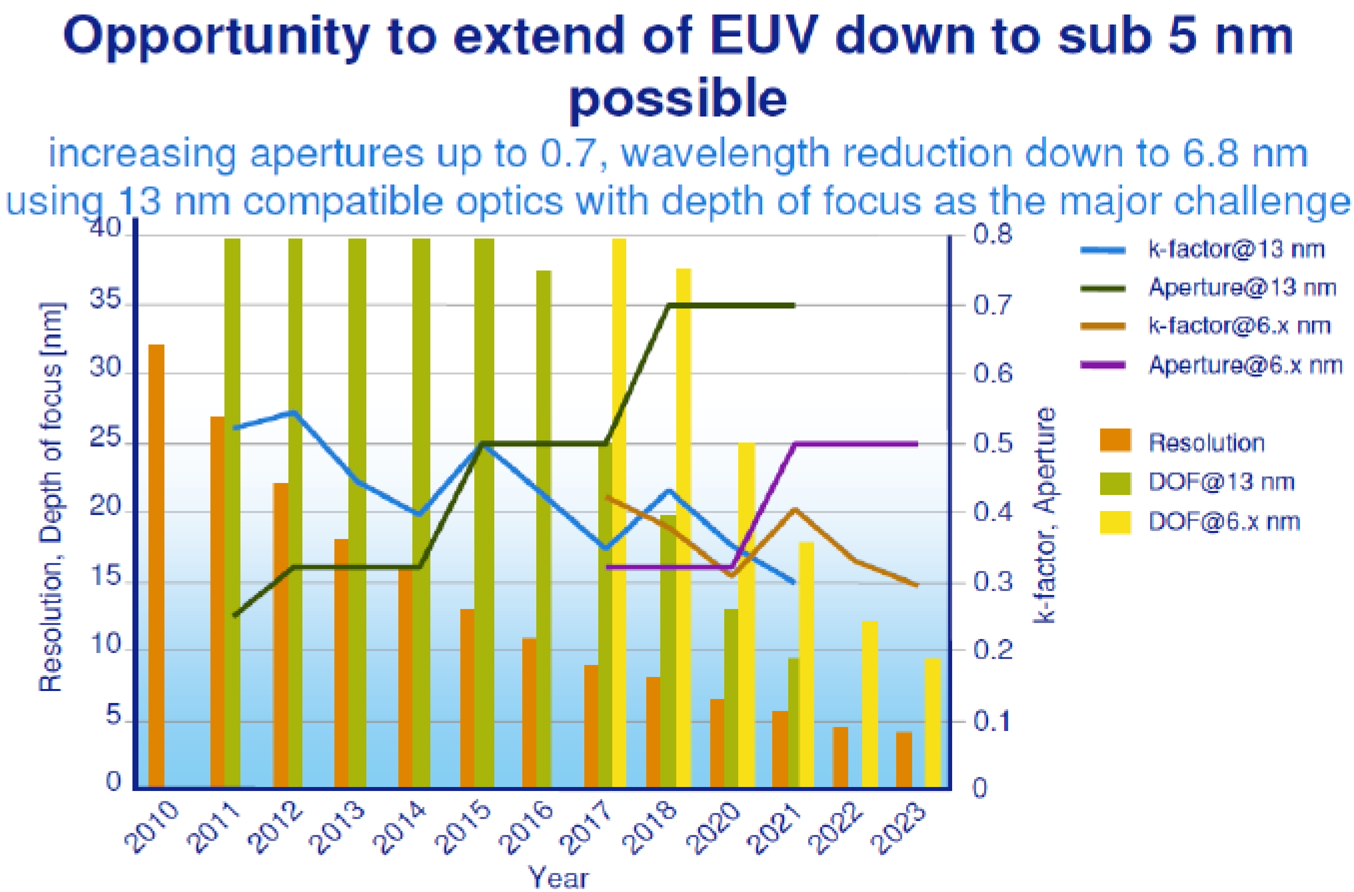
22 nm-18 nm HP
NA 0.33
ASML 3300B

16 nm-11 nm HP
NA>0.4
Nikon (Planned)

11 nm-8 nm HP
NA 0.33
λ = 6.7 nm!

Refs: ASML and Nikon Presentations

EUVL can extend to < 5 nm Resolution!

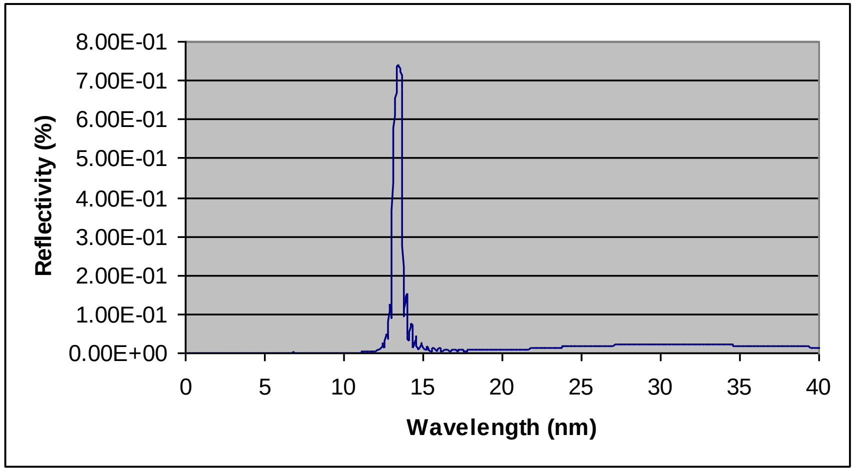


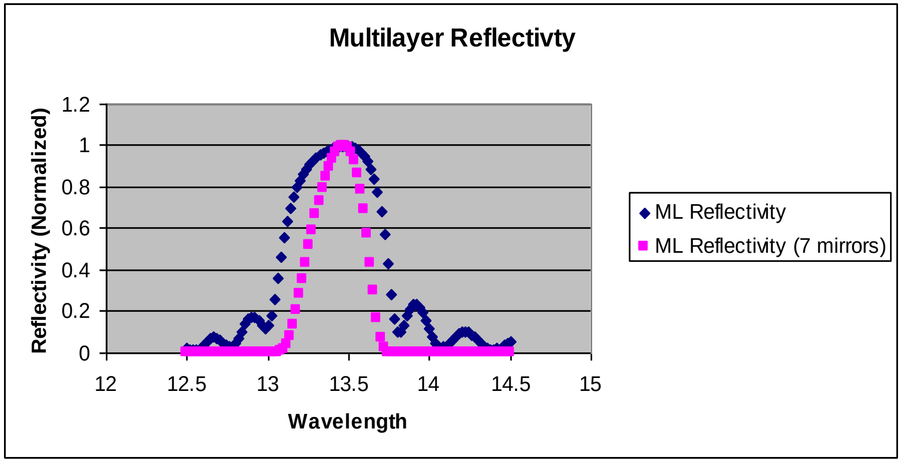
ASML presentation: 2010 International Workshop on EUV Sources, Dublin, Ireland

Introduction to EUV Lithography:

Why 13. 5 nm?

Si/Mo Multilayer mirrors (ML) offer a narrow band-pass filter, centered at 13. 5 nm, with peak reflectivity ~ 70%





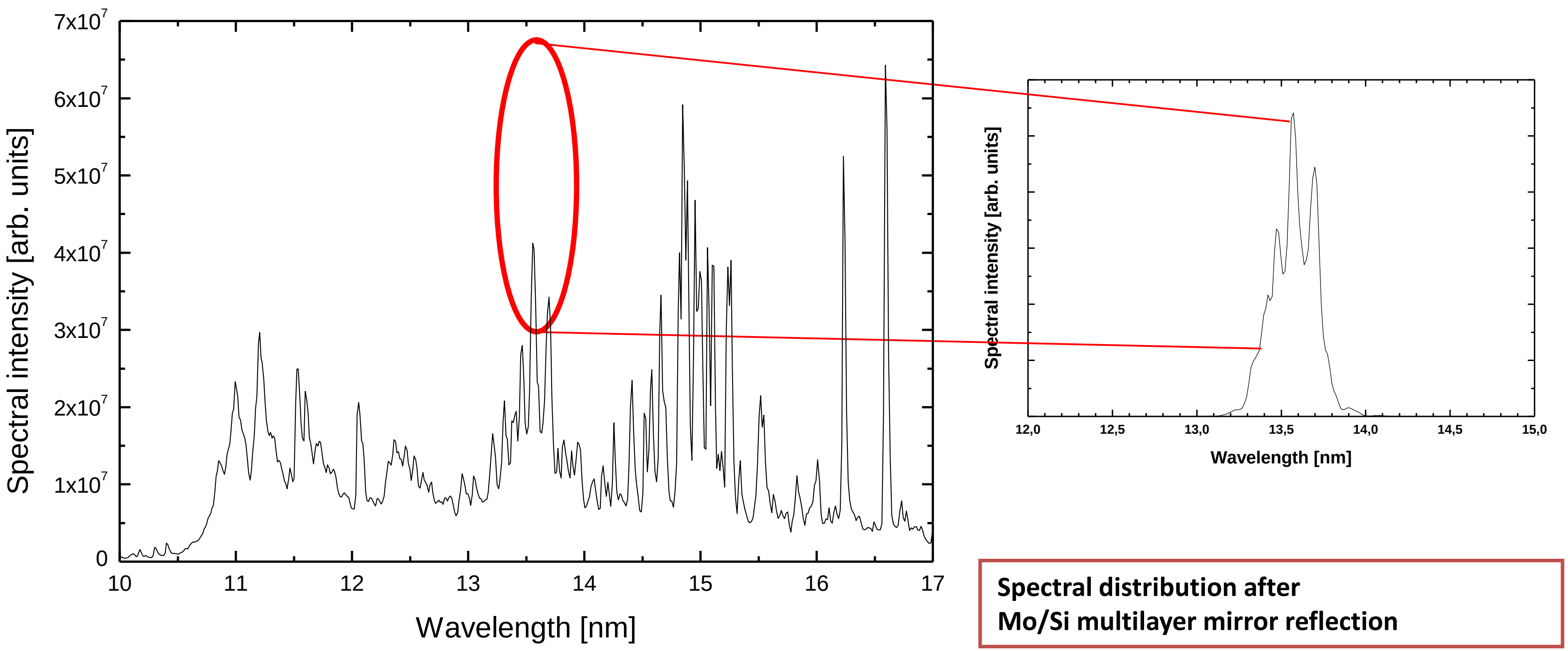
Si/Mo ML Reflectivity
0.1- 40 nm range

Si/Mo ML Reflectivity
Note narrowing of band pass
After seven reflections

Ref: http://www.cxro.lbl.gov

Introduction to EUV Lithography: Why 13. 5 nm?

ML reflects only wavelengths around 13.5 nm – converting Multi wavelength Xe spectra to narrow band. Filter function works well around 13.5 nm !



Spectral distribution after Mo/Si multilayer mirror reflection

Data Source: XTREME´s DPP Xenon Source

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EUVL scanner uses ML Mirrors (instead of lenses)

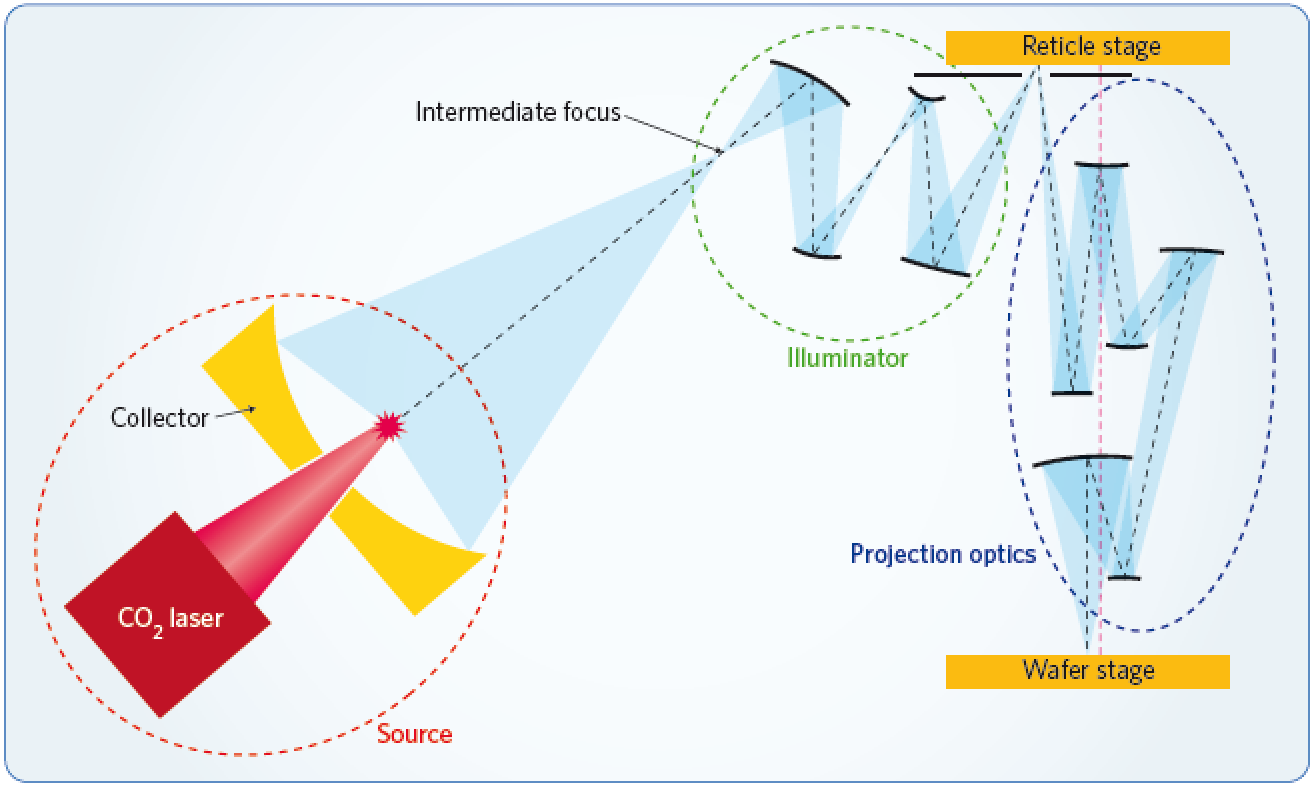


Figure 2 | Because all matter absorbs EUV radiation, the optics for collecting the light (collector), conditioning the beam (illuminator) and pattern transfer (projection optics) must use high-performance molybdenum-silicon multilayer mirrors, and the entire optical path must be housed in a near-vacuum environment.

EUVL is Optical Lithography with following key differences from current Lithography :

- EUVL uses plasma sources (radiating at 13.5 nm) instead of Excimer lasers (193 nm) for high volume manufacturing
- 13.5 nm light is readily absorbed therefore
  - EUVL scanners use reflective instead of refractive optics
    - EUV Optics and Reticles are Reflective multilayer mirrors
  - Entire EUVL scanner is kept in a high vacuum
- EUVL is the patterning technology for 32 nm half pitch and below.
  - Resolution = k_1 X Wavelength/Numerical Aperture
    - k_1= 0.4, NA =0.25 NA, resolution = 22 nm
    - k_1= 0.32, NA =0.45 NA, resolution = 10 nm

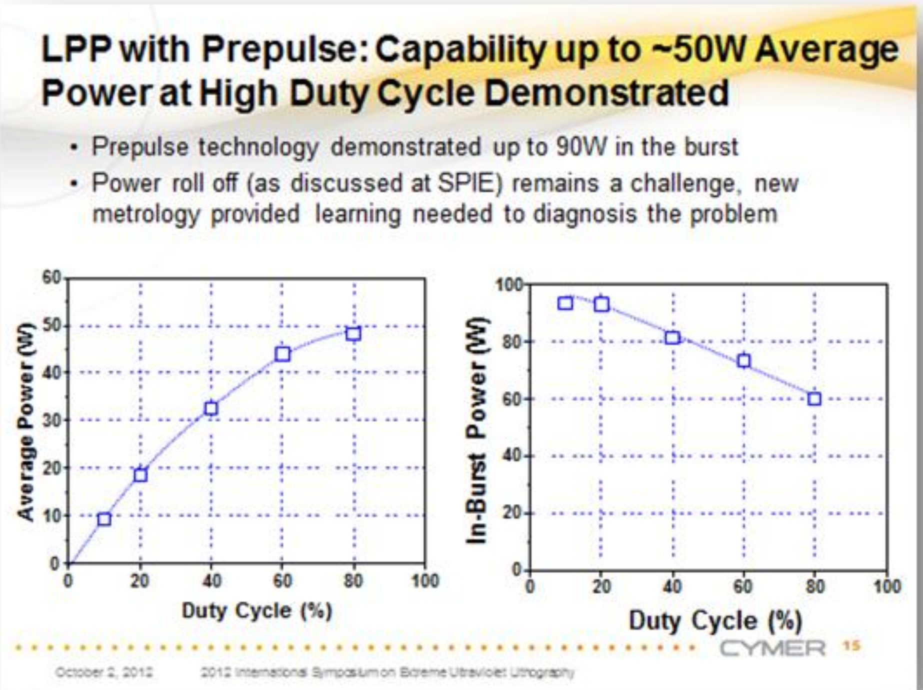
Outline

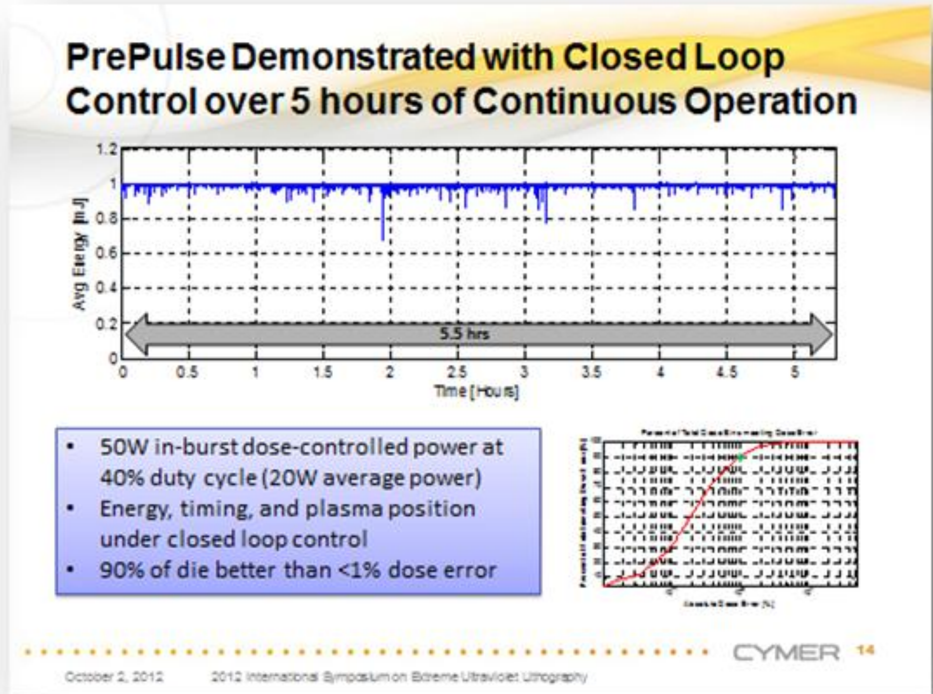
- Introduction to EUV Lithography
- Technical Status and Challenges
  - Source
  - Mask
  - Optics
  - Resist
  - Scanner
- Summary

EUVL Technology Status

EUV SOURCE STATUS

Sn LPP (Cymer): 50 W Av. Power Feasible with <1% dose error





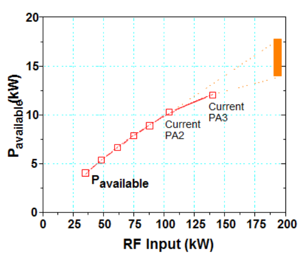
Special thanks to David Brandt

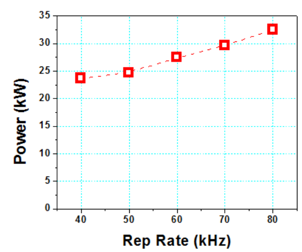
Source: V. Banine, 2012 Source Workshop

Sn LPP (Cymer): LPP Scaling – Promise of Scaling to 250 W

Power Scaling to 250W using CO_2 Laser Power, Conversion Efficiency and Repetition Rate

	Pilot 7	LT1	HVM II: 70W	HVM II: 125W	HVM II: 160W	HVM II: 250W
EUV in-burst power	40W	140W	70W	125W	160W	250W
EUV average power	32W	5W	70W	125W	160W	250W
Duty Cycle	80%	3%	100%	100%	100%	100%
Drive Laser	17kW	24kW	20kW	31kW	31kW	43kW
CE	1.1%	2.9%	2%	2%	2.5%	3%
Dose Control Margin	35%	NA	30%	20%	20%	20%

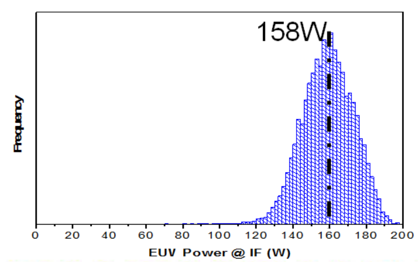


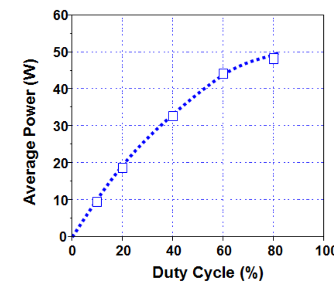


EUV Power Scaling Baseline

Low-Duty-Cycle Demonstration Status (LT1)	
Expose power (calc.)	140W
Raw power (mean)	158W
Raw power	190W
CO_2 power	24kW
Test length	>15min
Duty Cycle	3%

High-Duty-Cycle Demonstration Status (P7)	
Expose power (calc.)	40W
Raw power (mean)	60W
Raw power (peak)	70W
CO_2 power	17kW
Test length	~10min
Duty Cycle	80%





LPP shows potential of scaling in low duty cycle experiments

Special thanks to David Brandt

Source: V. Banine, 2012 Source Workshop

Sn LPP (Gigaphoton): 20 W with 5% CE demonstrated. 50 W Planned

GIGAPHOTON

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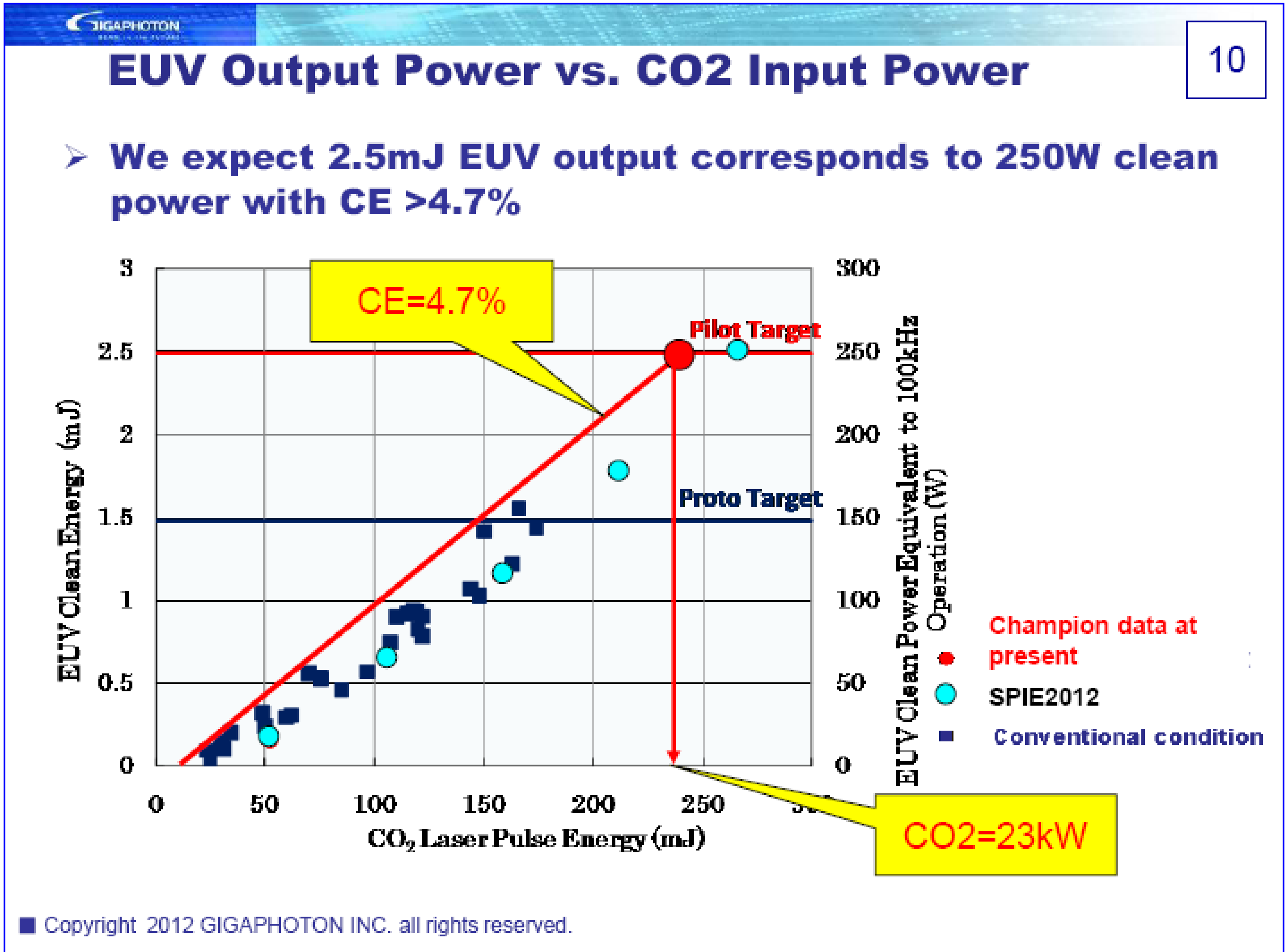
Summary

- 1st generation integrated setup LPP source (ETS) and 10 Hz device:
  - Smaller droplet (droplet size reduction from 60µm to 30 µm) extends operation time to 7 hours around 20W(clean power @I/F, 5%duty) level operation.
  - 10Hz experiment proved debris mitigation concept experimentally.
    That is proper pre-ionization and main ionization make >93% ionization. This technology enables clean light source in combination with magnetic field.
  - 10Hz experiment clarify CE (Conversion Efficiency) improvement, with <20µm droplet we found the region where CE >4.7% and perfect vaporization are simultaneously possible.
- 2st generation LPP source (GL200E):
  - Concept of design and outline is reported.
  - Our final goal of GL-200E is 250W and the feasibility is supported by high CE experimental data.
  - We observed 1st EUV light on proto source with 18W equivalent level at present. Next target is 50W level demonstration by 4Q 2012.

Source: H. Mizoguchi, 2012 EUVL Workshop

Sn LPP (Gigaphoton): Focus on increasing CE and debris control

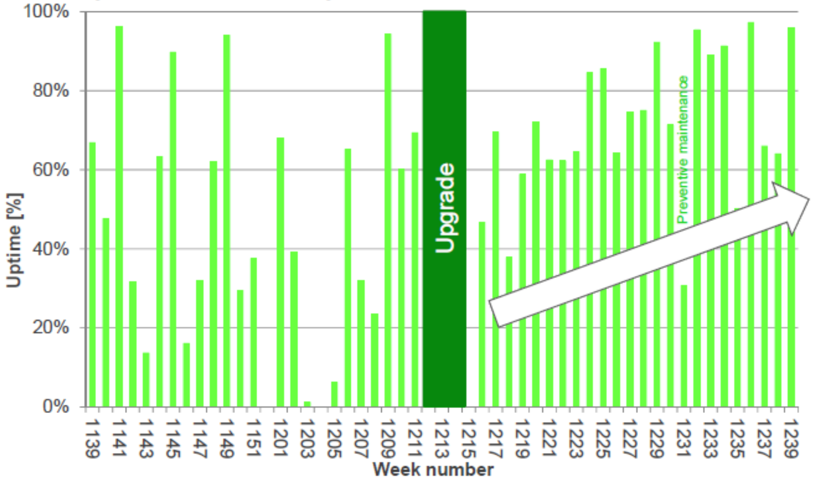


Source: H. Mizoguchi, 2012 EUVL Workshop

Sn DPP (Ushio): Upto 90% Uptime at ~ 7W source for NXE 3100

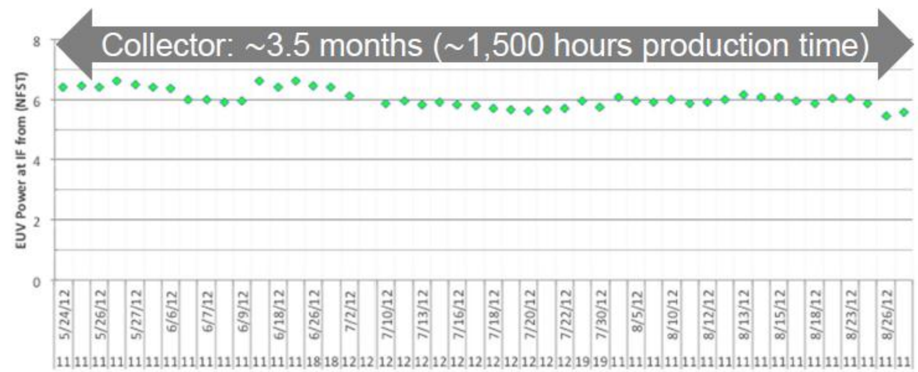
After Upgrade, Ushio 1 Uptime Has Steadily Increased …

- Recently, uptime exceeds 90% (13 wk average now exceeds 75%)
- Volatility has also drastically decreased



Long Collector Lifetime Is Achieved

- Power at IF is stable over the collector life



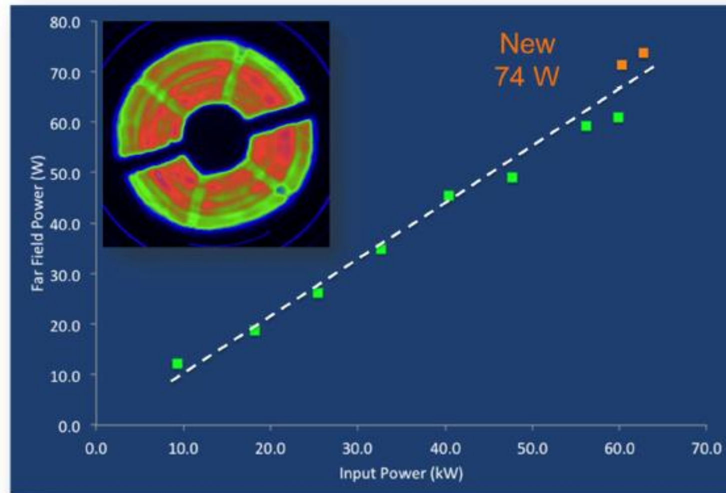
Special thanks to Rolf Apetz

Source: V. Banine, 2012 Source Workshop

Sn DPP (Ushio): 74 W potential!

Just In:

New Record 74 W After IF



Burst mode
200 ms / 12% DC

Pulse energy
3-4 J

1 hour run at 74W

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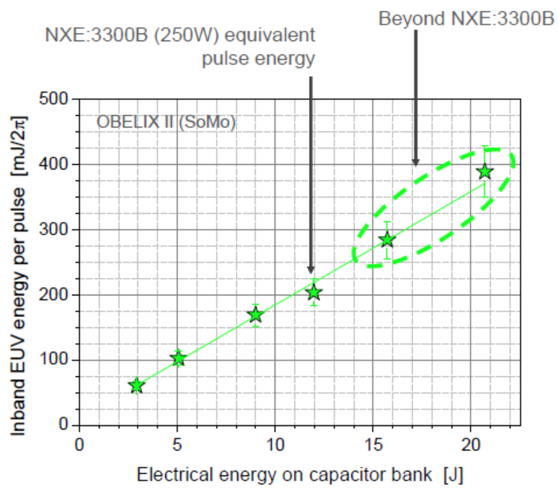
LDP Pulse Energy Scalability

- LDP's long term pulse energy scalability is proven BEYOND the requirements for NXE:3300B (250W)



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Please visit Poster P-SO-05 Felix Kuepper, Fraunhofer ILT

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DPP shows potential of scaling in low duty cycle experiments

Special thanks to Rolf Apetz

EUV LITHO, INC.

Source: V. Banine, 2012 Source Workshop

EUV Source Technology Status (Oct. 2012)

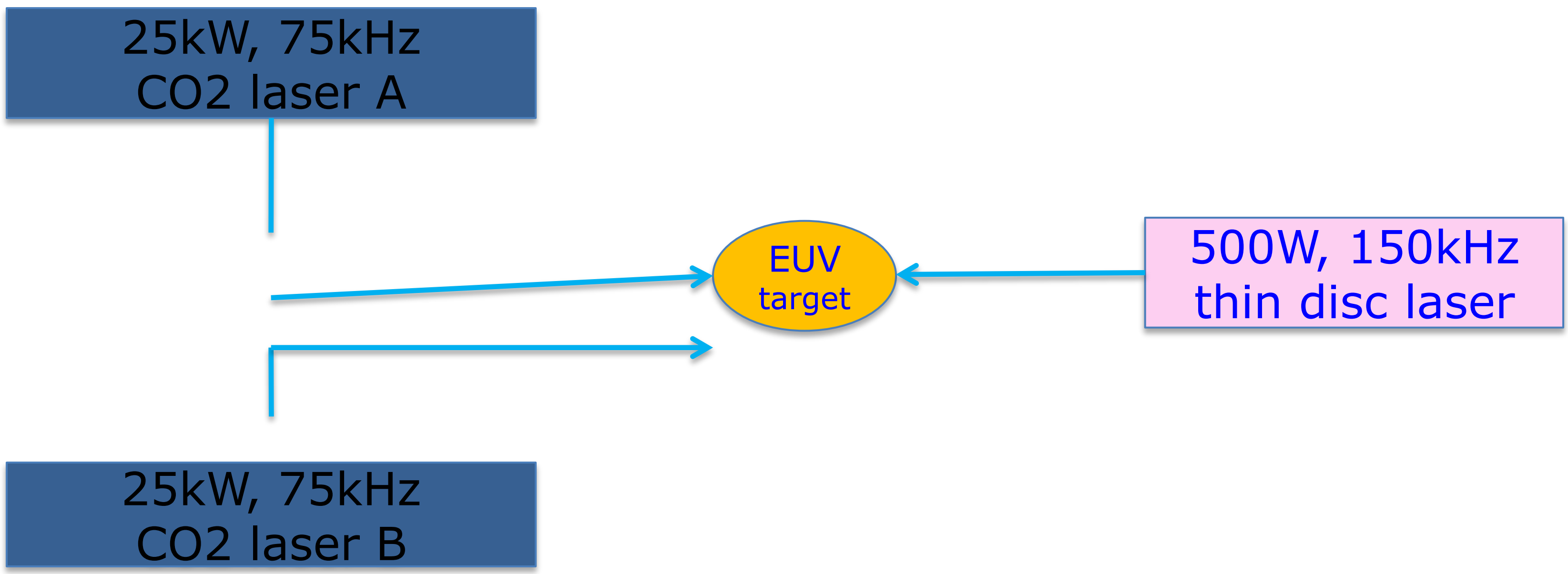
- LPP (Cymer) – Sn LPP
  - Shipped Six SoCoMo to ASML for insertion in β scanners (Model NX3000) and are now operational in field
  - ~10 W Exposure power at with <1% stability and 50% source availability. 50 W potential demonstrated
- LPP (Gigaphoton) – Sn LPP
  - ETS system - 20 W average power with 30 micron droplets and 5 % CE, with > 7 Hour of operation
  - R&D results show 2.5 mJ pulse energy (corresponding to 250 W) and 5 % CE with < 20 micron droplets and 93% debris mitigation
- DPP (Xtreme – USHIO)- Sn DPP
  - 7 W Exposure power at 100 % duty cycle with >75% availability
  - 75 W potential demonstrated

EUV Litho, Inc.

1000 W Sn LPP Source is Feasible!

Ref: Akira Endo, 2012 Source Workshop

Configuration of 150kHz, 1kW EUV source



- Speedup of 10μm diameter Tin droplet to 150m/s
- Dual CO2 laser modules are operated for 150kHz
- Sn Cluster formation by picosecond solid state laser
- Laser resonant ionization of neutrals

Challenges to Conventional Scaling of LPP

- CE increase viability at higher powers? (GPI @ SPIE 2012 reported 5%)
- Laser power scaling or multiplication
- Maintaining cold gas buffer for lifetime of the mirror at the 3-4x increase of power load
- Maintaining lifetime of collector at increased (3x-4x) Sn consumption (Is GI collector a viable idea in this case?
- Droplet generator scalability to higher frequencies?

Source: V. Banine, 2012 Source Workshop

Challenges to Conventional scaling of DPP (LDP)

- Is CE increase an option?
- Will discharge heads still work at this power (e.g. Sn evaporation and glow mode) or jets is a way (Koshelev et al SPIE 2012)
- How to scale foil trap when > ½ MW is dissipated at a short distance (increase the distance -> collector size and track length)

Source: V. Banine, 2012 Source Workshop

List of Source R&D Topics

- How to increase and sustain CE increase
- Understanding Limits of CE and power
- New source configurations to enable power scaling of DPP and LPP
- Debris mitigation strategy for high power sources
- High brightness sources for metrology – development and understanding limits
- Ps, 500 W lasers for pre pulse for Sn LPP
- Development of 25-100 kW, pulsed CO_2 laser modules
- Development of BEUV sources
- Development of non-plasma sources for HVM and BEUV

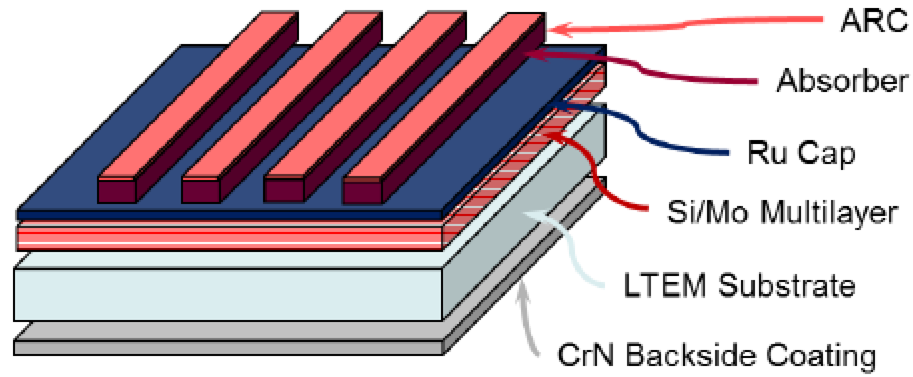
EUVL Technology Status

EUV MASK STATUS

Hard EUV Mask Blank Challenges

Substrate and Blank

- Absorber/ARC Stack
  - Optical Properties at EUV
  - Properties at Inspection Wavelengths
  - Particle Defects
  - Etch Performance



- Ru Cap
  - Particle Defects
  - Film Loss from Etch
  - Metrology
- Multilayer
  - Particle Defects
  - Uniformity
  - Reflectivity and Centroid Wavelength
  - Metrology (Defect Detection)

This is difficult!

- Substrate
  - Thermal Properties
  - Particle and pit defects
  - Subsurface polishing damage
  - Flatness and Surface Roughness
  - Metrology (Defect Detection)
- Backside Coating
  - Electrical Properties
  - Defectivity

Source: S. Wurm, 2012 Semicon West

EUV Substrate and Blank Specification

Technical Requirements & Performance

SEMATECH

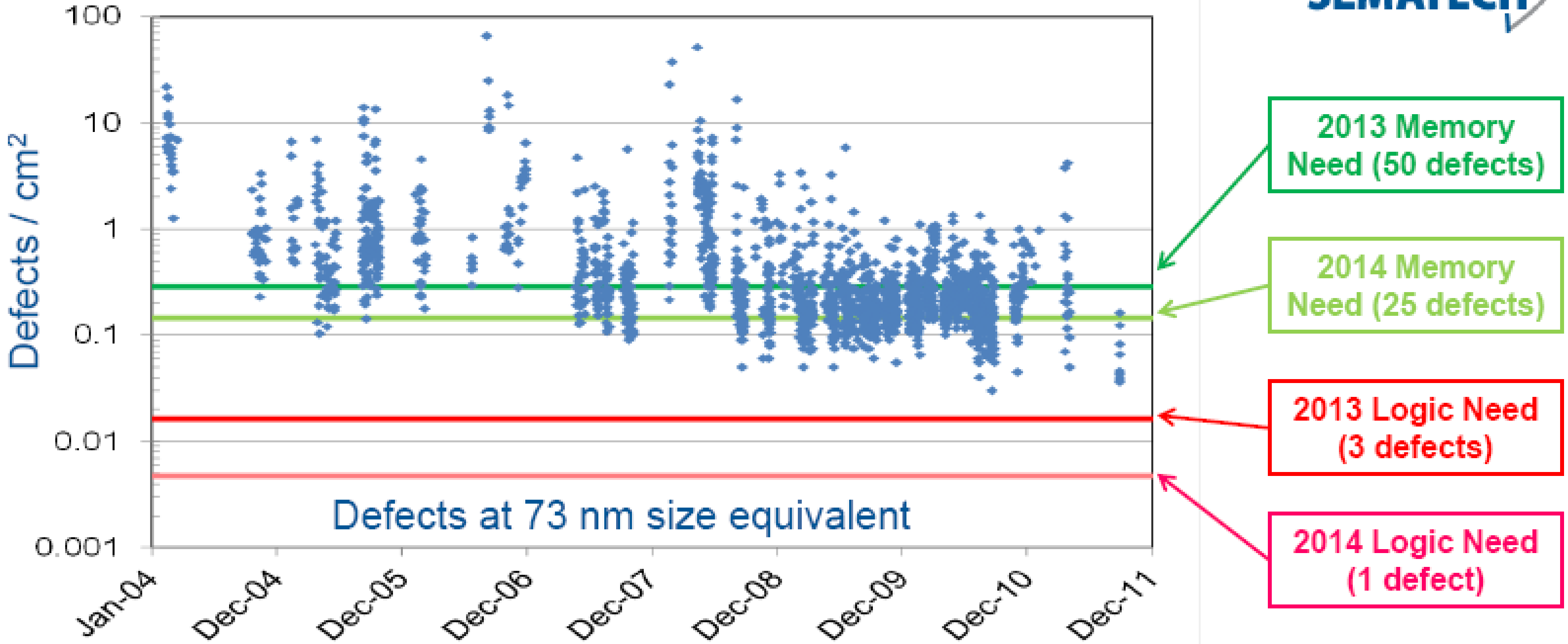
Material	Property	Spec	Performance
Substrate*	Mean CTE	± 0.5 °C	± 0.4 °C
	CTE Variation	< 6 ppb/°C	4 ppb/°C
	Frontside (FS) flatness (PV)	≤ 30nm	50 nm
	Backside (BS) flatness (PV)	≤ 30nm	84 nm
	FS Roughness ($\lambda_{spatial} \leq 10$ µm)	≤ 0.05 nm RMS	0.15 nm RMS
	FS Local slope (400 nm ≤ $\lambda_{spatial} \leq 100$ mm)	< 1 mrad	Measurements in process
	BS Roughness (50 nm ≤ $\lambda_{spatial} \leq 10$ µm)	≤ 0.50 nm RMS	Not critical
Mask Blank	Defect density @ 50nm (SiO_2 Eq.)	≤ 0.008	0.121
	Min. Peak reflectivity	> 63.8%	64.1%
	Peak reflectivity uniformity	0.3%	0.3%
	Centroid wavelength	± 0.03nm	0.00nm
	Centroid wavelength uniformity	0.06nm	0.02nm

**Substrate does not have a defect specification*

Source: S. Wurm, 2012 Semicon West

EUV Litho, Inc.

Defect Density Trend



- Memory requirements
  - Overall defect counts are meeting requirements
  - Large size "Killer" defects still present remain a concern for mask yield
- Logic requirements for 2013 not being met
  - Trend over the last 2 years looks positive to achieving these defect levels

Source: S. Wurm, 2012 Semicon West

Actinic Mask Inspection Tools Needed

Blank Inspection Sensitivity

Well characterize test mask for tool characterization

22nm hp

16nm hp

Cell #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Surf.W	1000	750	500	300	200	180	160	140	120	100	90	80	72	66	51	43
Surf.H	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.5	1.5	1.4	1.3	1.2	1.1	1.0
SEVD	151	124	95	68	52	48	44	41	37	32	30	27	24	21	18	15

BI sensitivity assessment

Currently existing DUV tools

Future actinic tools under development

- BI tools can support pilotline and early TD learning
- New actinic BI development to meet the need for HVM
  - EIDEC consortium; KLA 7XX partnership
  - Must detect amplitude defects

intel

2011 EUVS, Miami, FL

23

EUV Litho, Inc.

AIMS EUV Project Underway at Carl Zeiss: Tool to be Delivered by 2014

(Current Source brightness 8 $W/mm^2.sr$, min needed 30 $W/mm^2.sr$)

AIMS™ EUV Project

ZEISS

Sematech EMI (EUV mask infrastructure) consortium

Need: Clear vote from all IDMs/mask manufactures for the need on an AIMS™ EUV

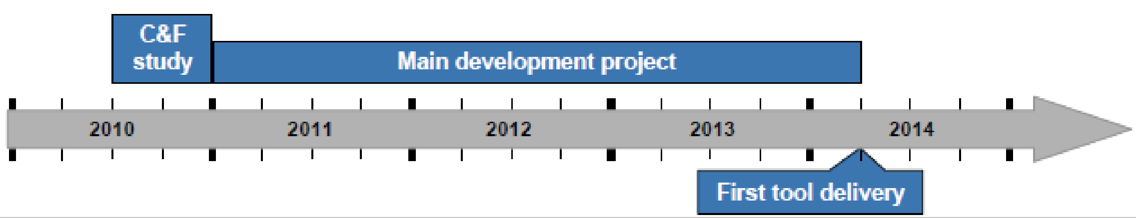
Phase 1: AIMS™ concept & feasibility (C&F) study

Structure: contract for C&F study between Sematech and Zeiss in place

Objective:
- define specification, timeline and project cost
- decide on technical concept
- finalize development contract for main project starting Jan 2011

Phase 2: Main development project

Prerequisite: - development contract signed by Dec 2010



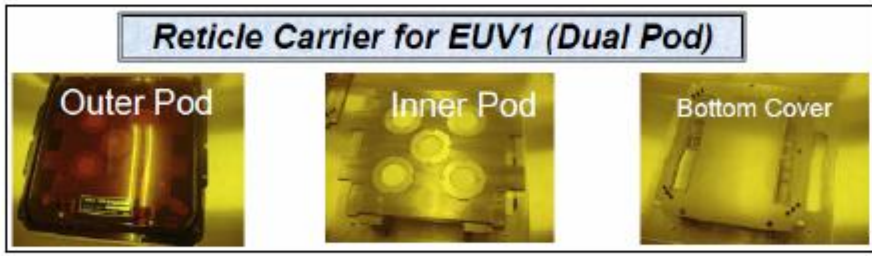
EUV Litho, Inc.

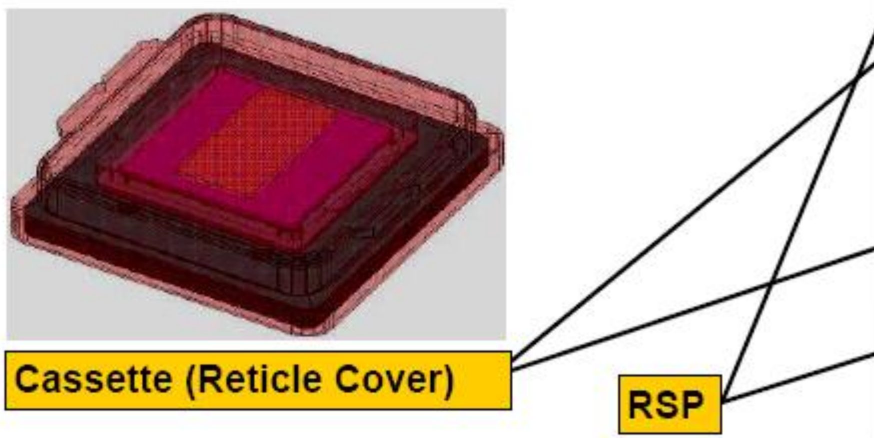
Reticle Particle Protection

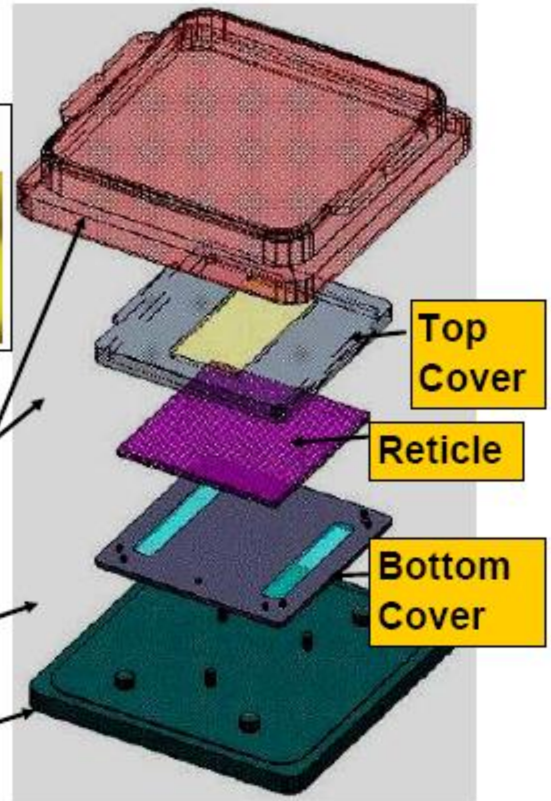
NIKON CORPORATION
Precision Equipment Company

1. Reticle in Cassette (RC) in Carrier (RSP200).
2. Cassette protects the reticle in load locks.
3. Top cover stays with reticle during in-tool handling.
4. Reticle remains in RC in library to protect against vacuum accidents and contamination.

Dual Pod Concept by Canon and Nikon

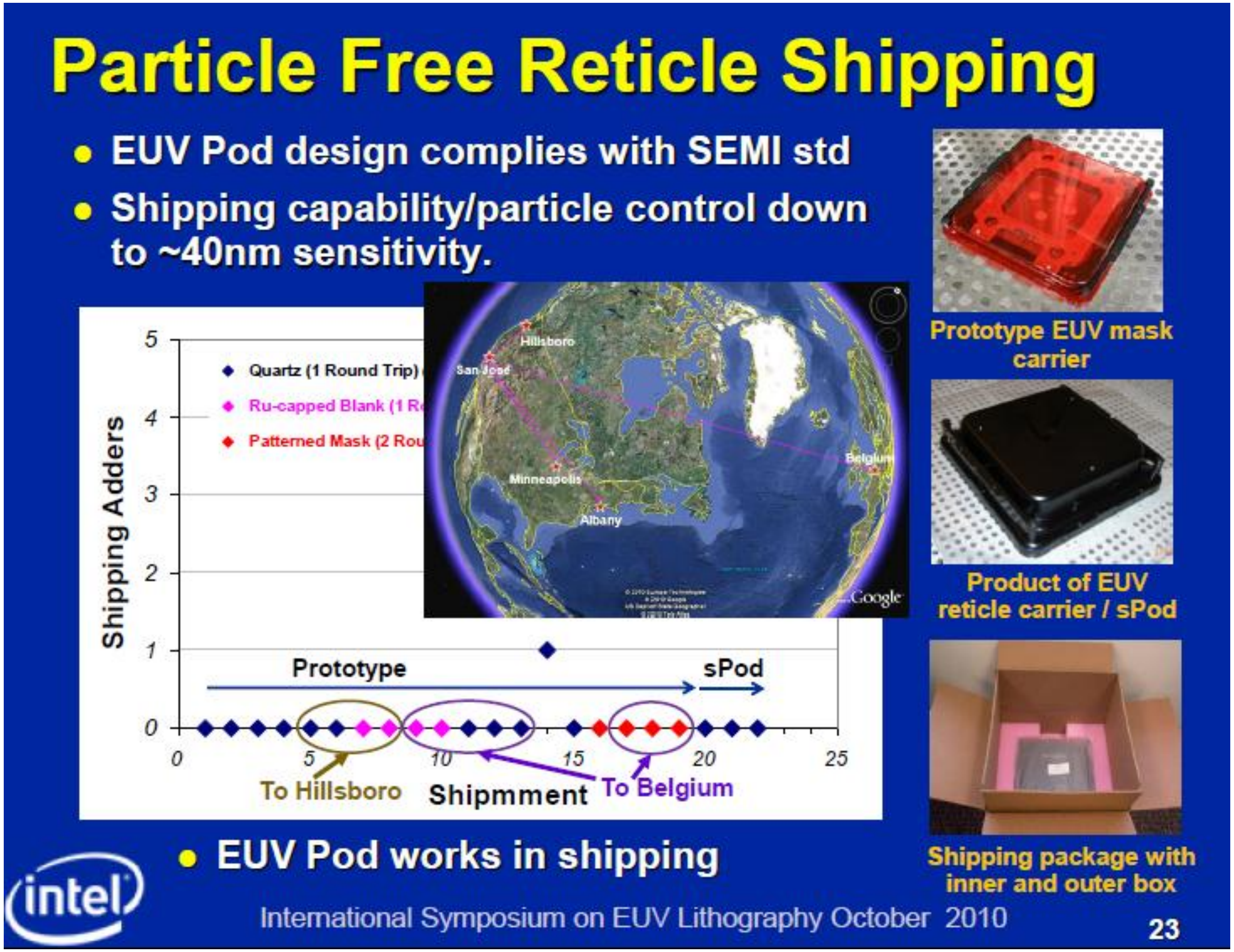






SEMI standardization completed.

Particle Free Reticle Shipping: EUV POD Works!



Zhang et al, EUVL Symposium 2010

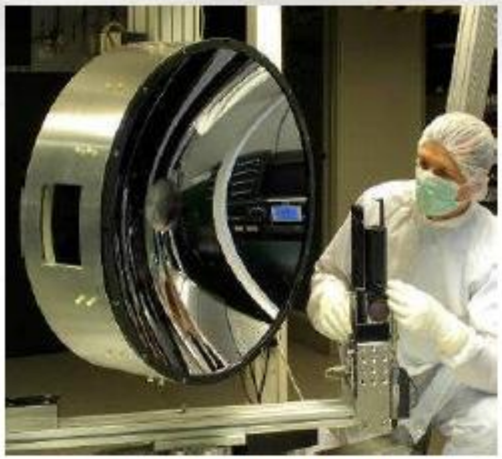
EUVL Technology Status

EUV OPTICS STATUS

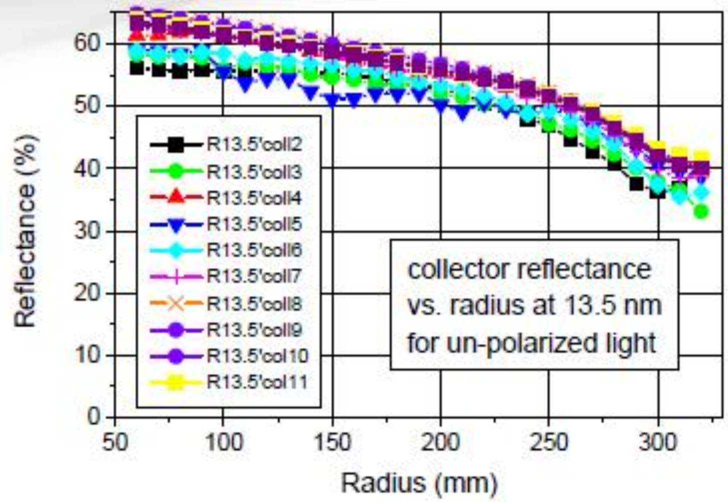
EUV Source Collector Optics: 52% Average reflectivity

5sr Collector Reflectivity Measurements

Average reflectivity >50%, Measurements of 10 Collectors



Mapping surface of collector



- **52.1% average area-weighted reflectivity reached at 13.5 nm**
  - Collector reflectivity measured at PTB using synchrotron radiation
  - Reflectivity for un-polarized light determined from data measured with s-polarized light

CYMER 21

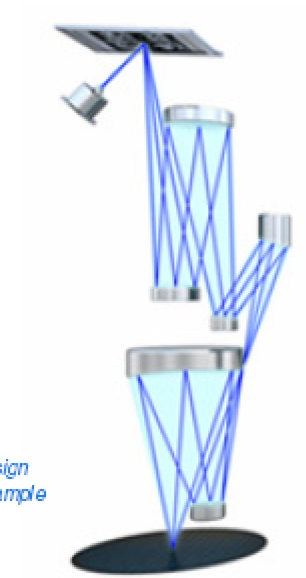
October 19, 2010 2010 EUVL Symposium, Kobe Japan

EUV Litho, Inc.

EUV Optics is in Production Phase

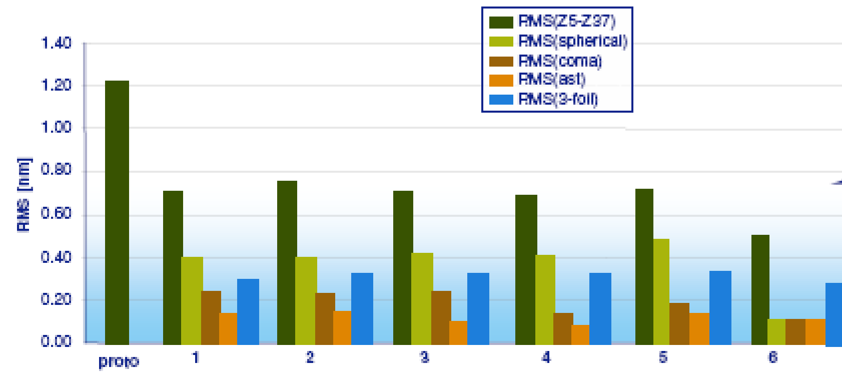
all NXE:3100 lenses are manufactured and qualified

Wave front qualified by EUV – interferometer

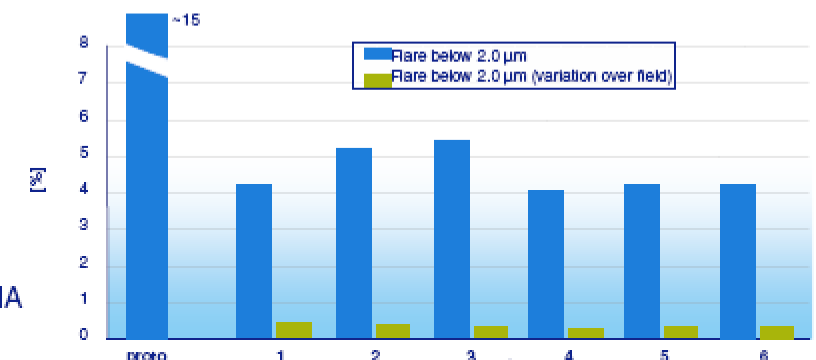


design example

- Field size: 26mm
- Chief ray at mask: 6°
- 4x reduction ring field design
- Design is extendable to higher NA



NXE:3100 lenses within flare specifications



Slide 6 | SPIE March 2011

ASML

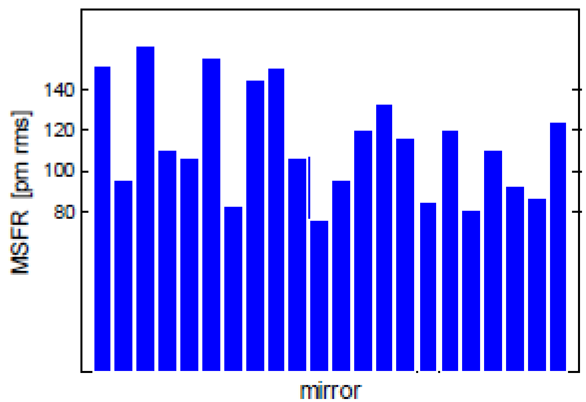
EUV Litho, Inc.

EUV Optics is in Production Phase

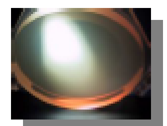
NXE:3300 – Improvements in mirror polishing allow for reduced flare on larger and more complex mirrors

ZEISS

3100 status



Improvement potential successfully demonstrated

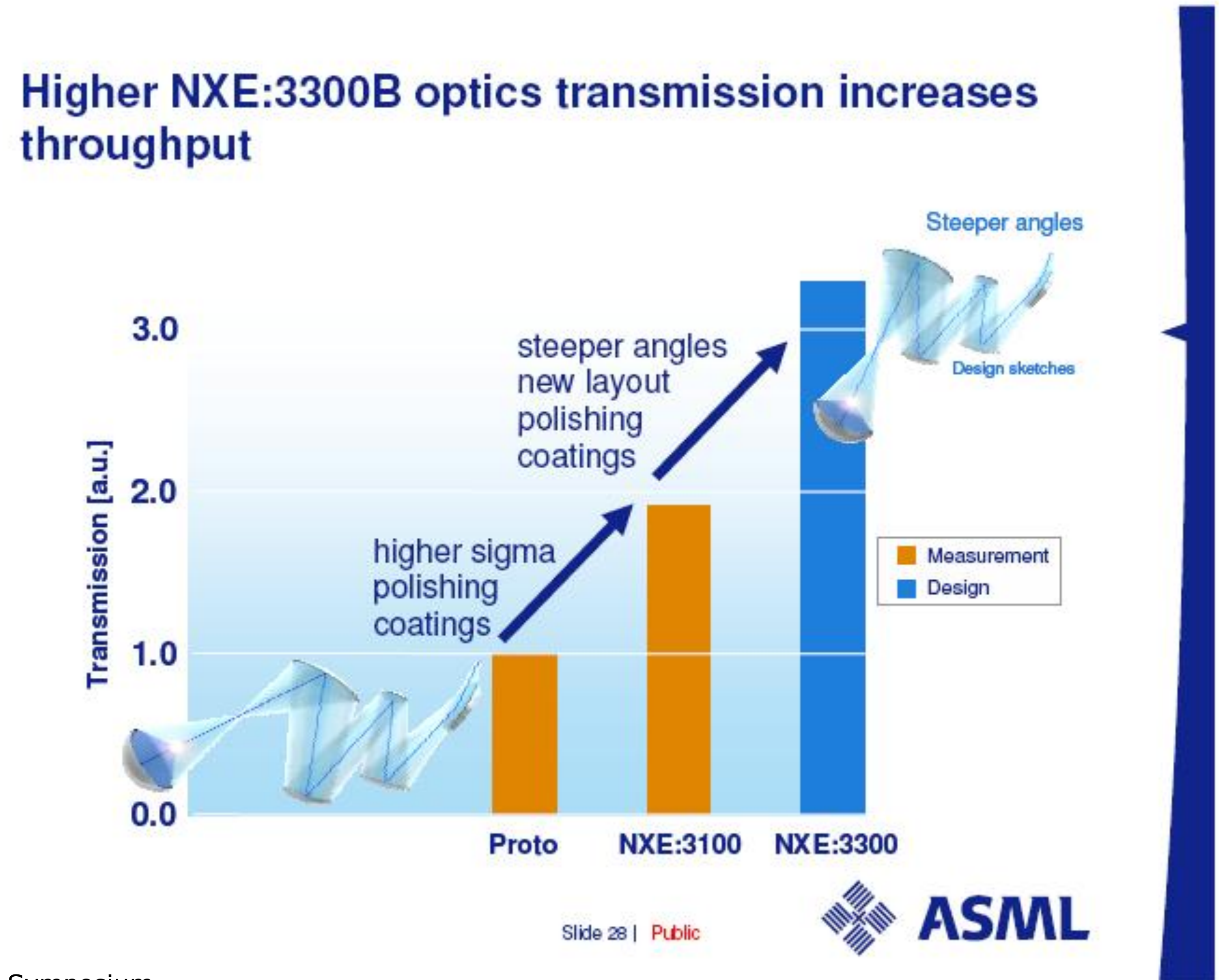


	Champion 1	Champion 2
MSFR	68 pm	59 pm
Figure and HSFR are in spec. as well		
Figure	45 pm	30 pm
HSFR	70 pm	95 pm

Further improvement potential for 3300 production demonstrated

EUV Litho, Inc.

3 x Transmission (and throughput) Increase Expected for NXE:3300B



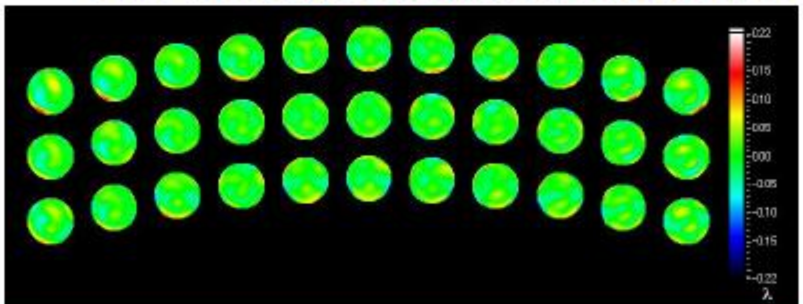
ASML: 2011 EUVL Symposium

Nikon: Optics ready for HVM

Optics Performance

NIKON CORPORATION
Precision Equipment Company

EUV1 PO: WFE and Flare Performance

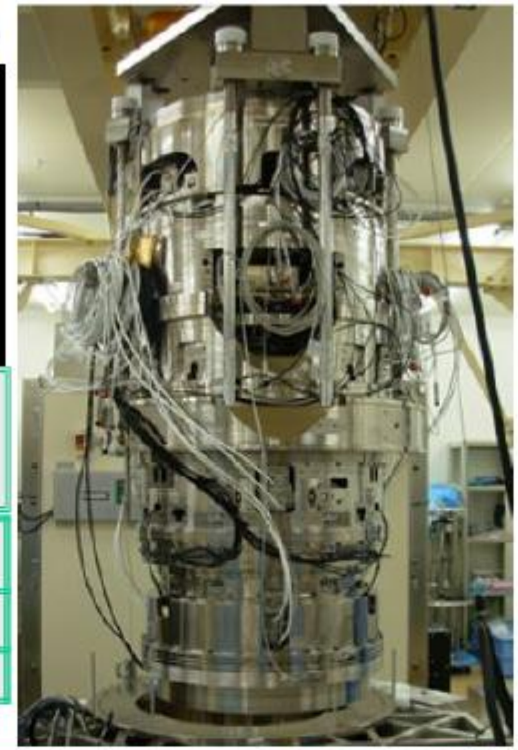


WFE: 0.4 nm RMS (average)

Min. 0.3nm RMS ~ Max. 0.5nm RMS

	Flare	Kirk flare (estimate/measure)
EUV1 PO#1	10%	15% / 16%
EUV1 PO#2	6%	8% / 8.5%

2μm Kirk pattern in bright field



- If all 6 mirrors assumed to have same MSFR and HSFR as those of the best mirror in PO#2 static Kirk flare will be reduced to 3.4% from 8%.

Refer to Proc. SPIE 7636, 763629 (2010) by M. Shiraishi, et al.

2010 EUVL Symposium @Kobe, Japan October 18, 2010

Slide 7
Slide 7

EUV Litho, Inc.

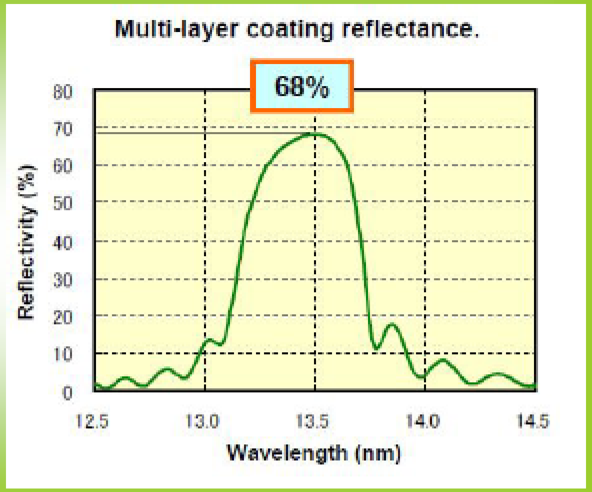
Nikon: Optics ready for HVM

Mirror fabrication technology

NIKON CORPORATION
Precision Equipment Company

Further improvement of MSFR, HSFR
⇒ Lower flare, Higher reflectivity

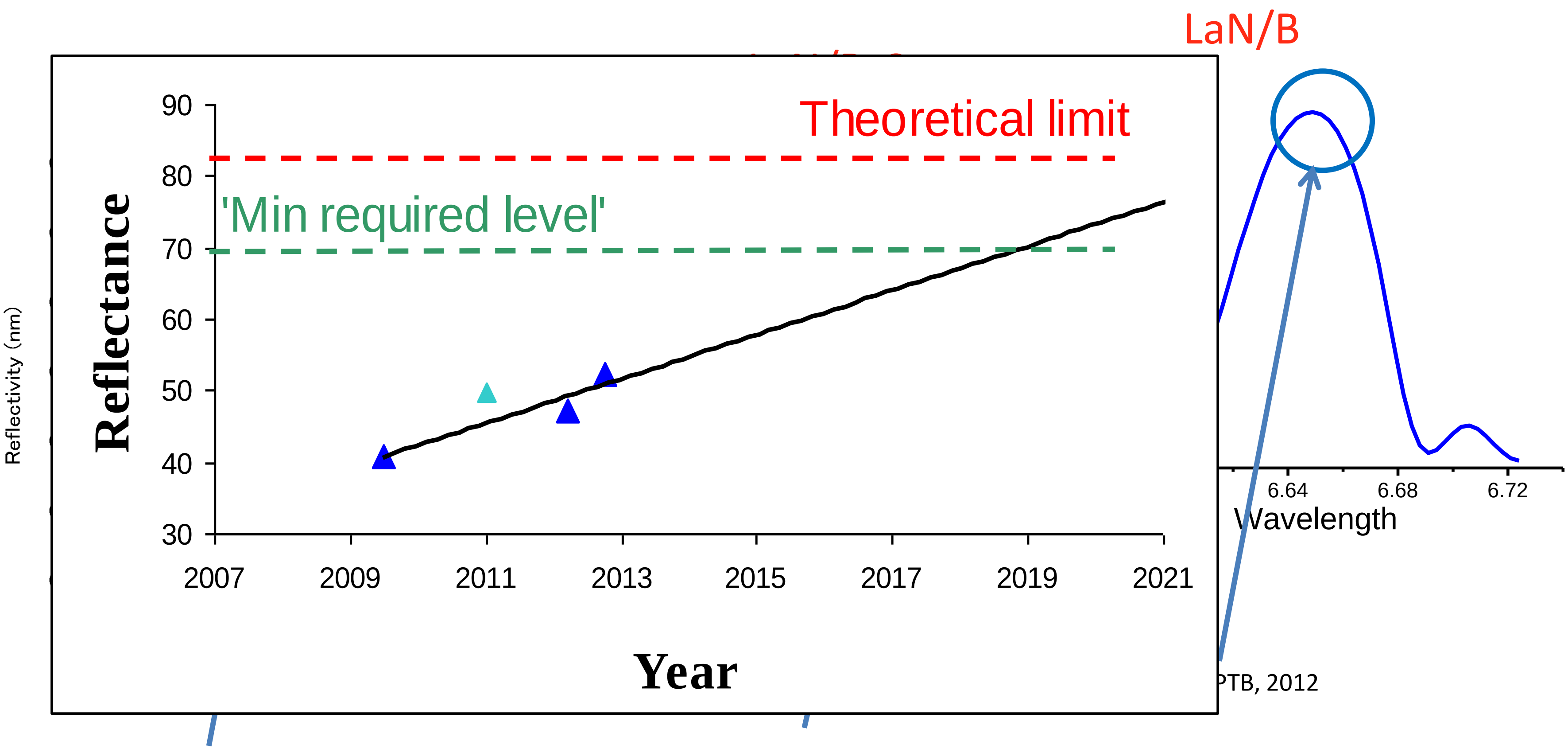
	MSFR (pmRMS)	HSFR (pmRMS)
PO#1	100~140	70~130
PO#2	70~130	70~120
2010	51	50



Nikon's optics fabrication technology can meet EUV HVM requirements.

2010 EUVL Symposium @Kobe, Japan October 18, 2010 Slide 9

Status of 6.776 nm BEUV ML Optics



49.83%

Q1 2012: 47.20%

Q3 2012: 53.6%

Rigaku Osmic® EUV Optics

Courtesy Platonov, OSMIC

FOM

FOM

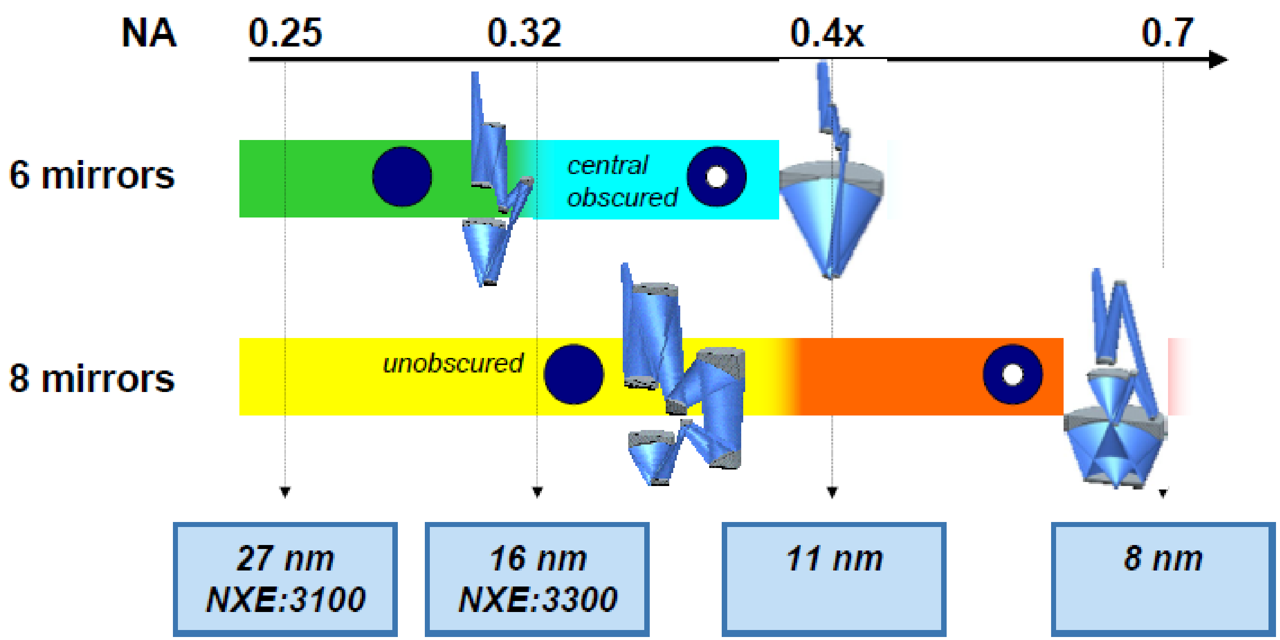
 Source: E. Louis, 2012 Source Workshop

EUV Litho, Inc.

Scanner Optics Designs Available for 8 nm Resolution

We see design solutions for high NA systems enabling 11 nm resolution and beyond

ZEISS



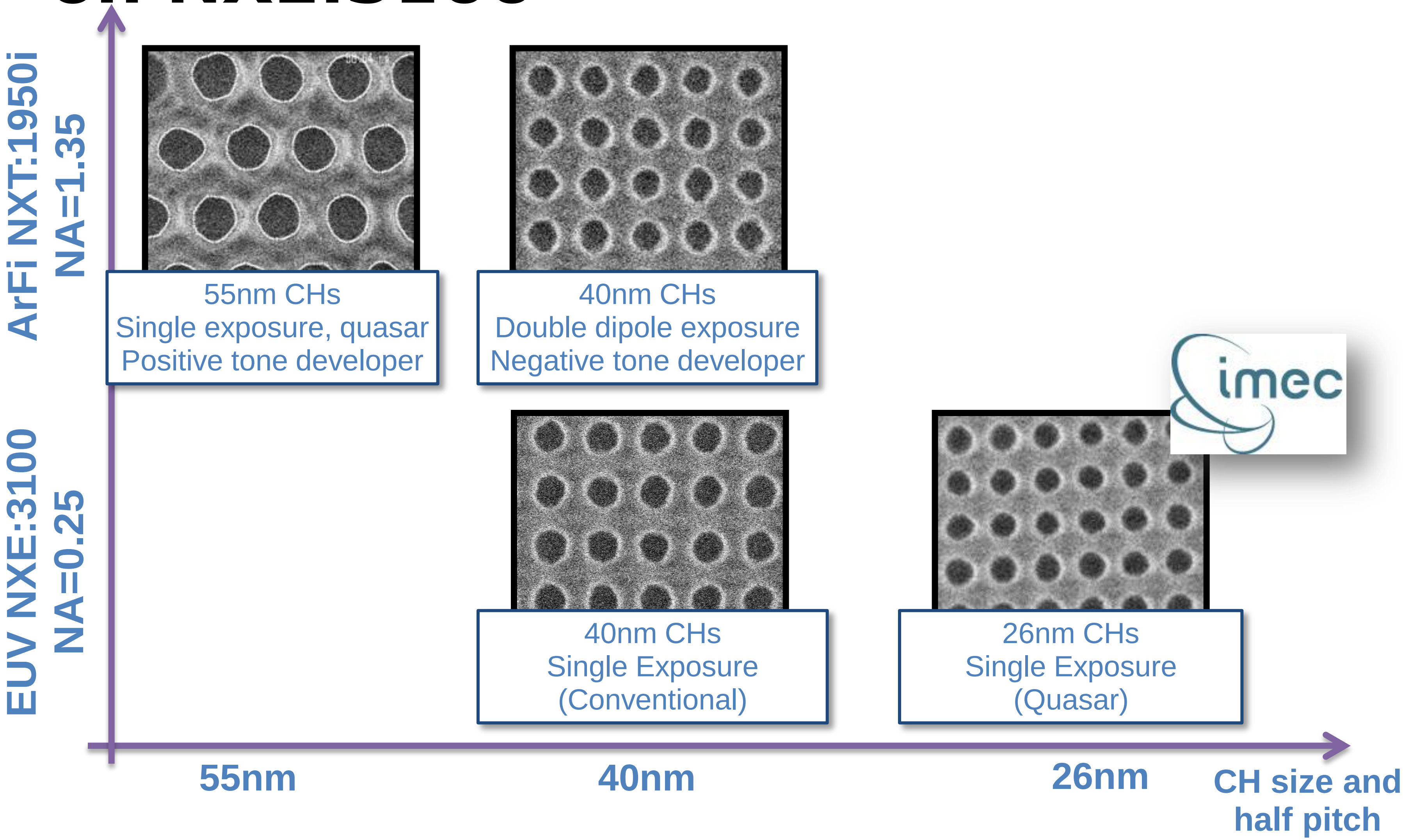
schematic designs – for illustration only.

W. Kaiser et al., SPIE 2008

EUVL Technology Status

EUV RESIST STATUS

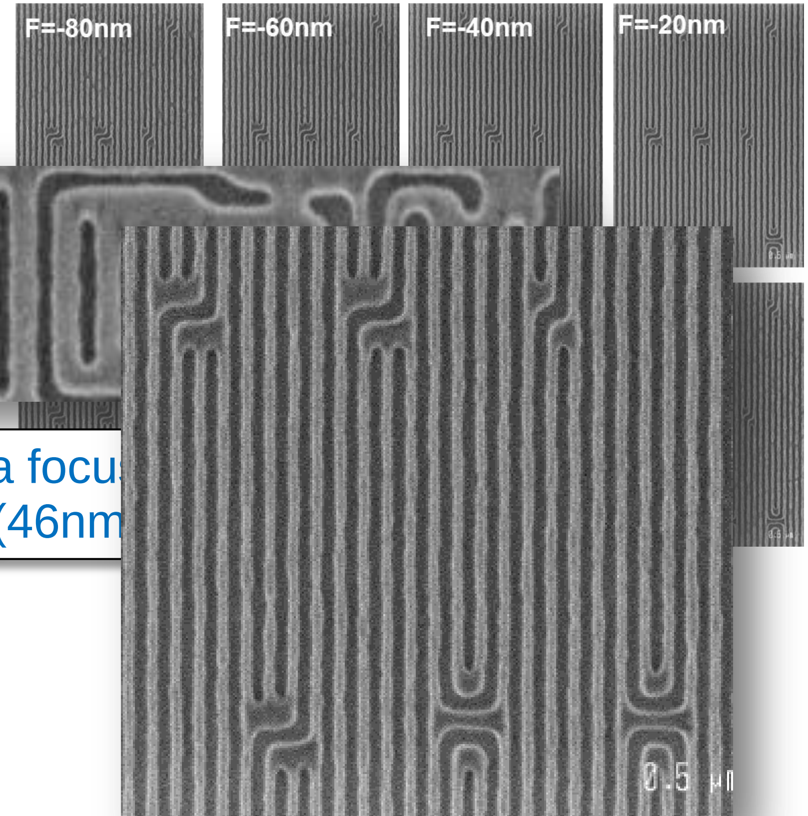
Dense CH imaging down to 26nm on NXE:3100



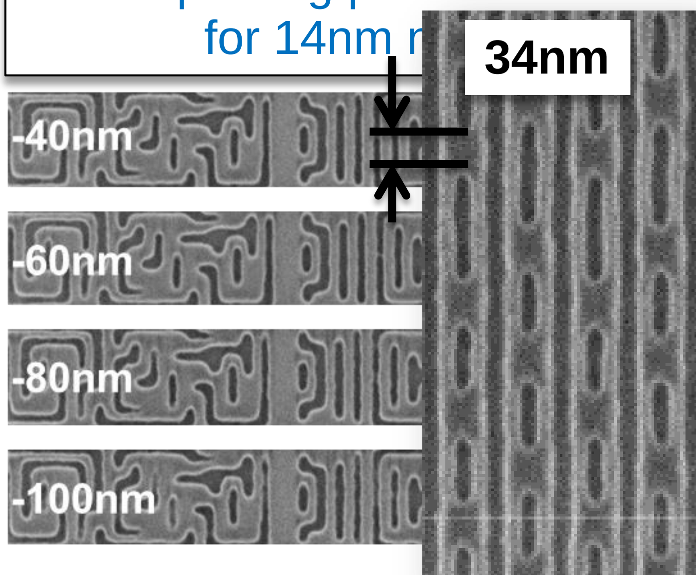
Source: V. Banine, 2012 Source Workshop

Single exposure 14nm node metal 1 features

Focus



Good printing performance through a focu
for 14nm r clip (46nm



Good printing performance for 14nm node Metal clip (44nm min. pitch) through a focus range of ~120nm

Source: V. Banine, 2012 Source Workshop

LWR remains the leading challenge for EUV resists

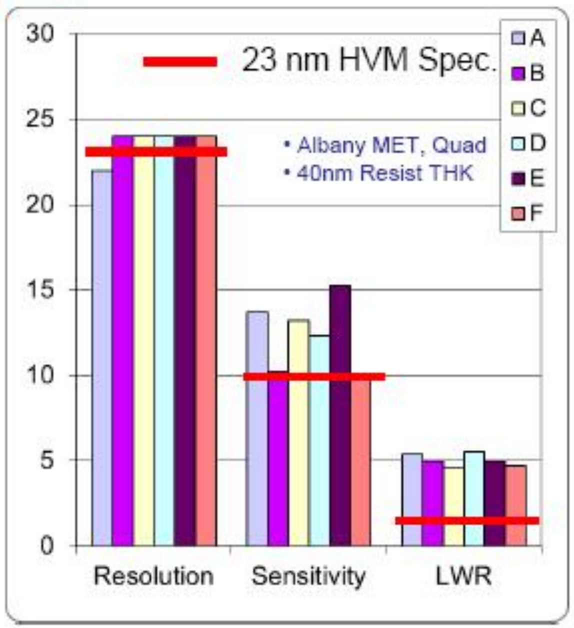
EUV Resist Performance Status

High Level Summary

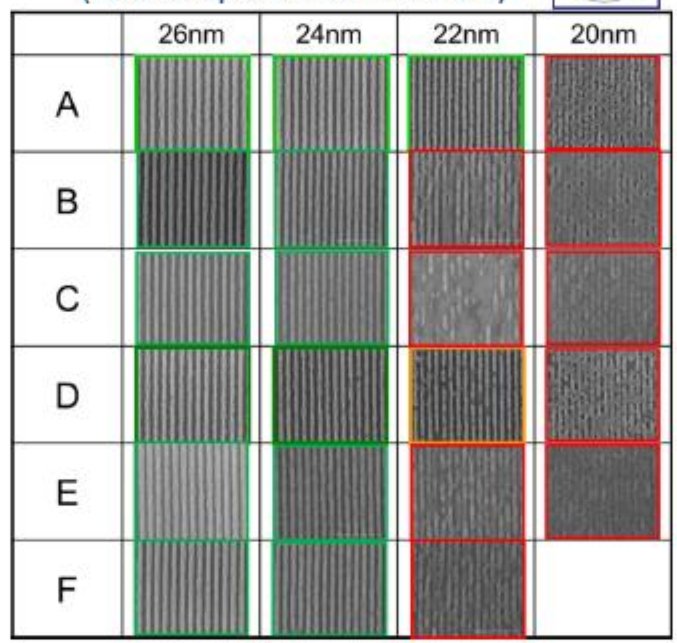
SEMATECH

Performance against key metrics

Goal 23 nm HP 10mJ/cm² 1.6 nm LWR



Best resist for each supplier (Quadrupole illumination)



- A number of suppliers are making progress with sensitivity and resolution but LWR has not improved.

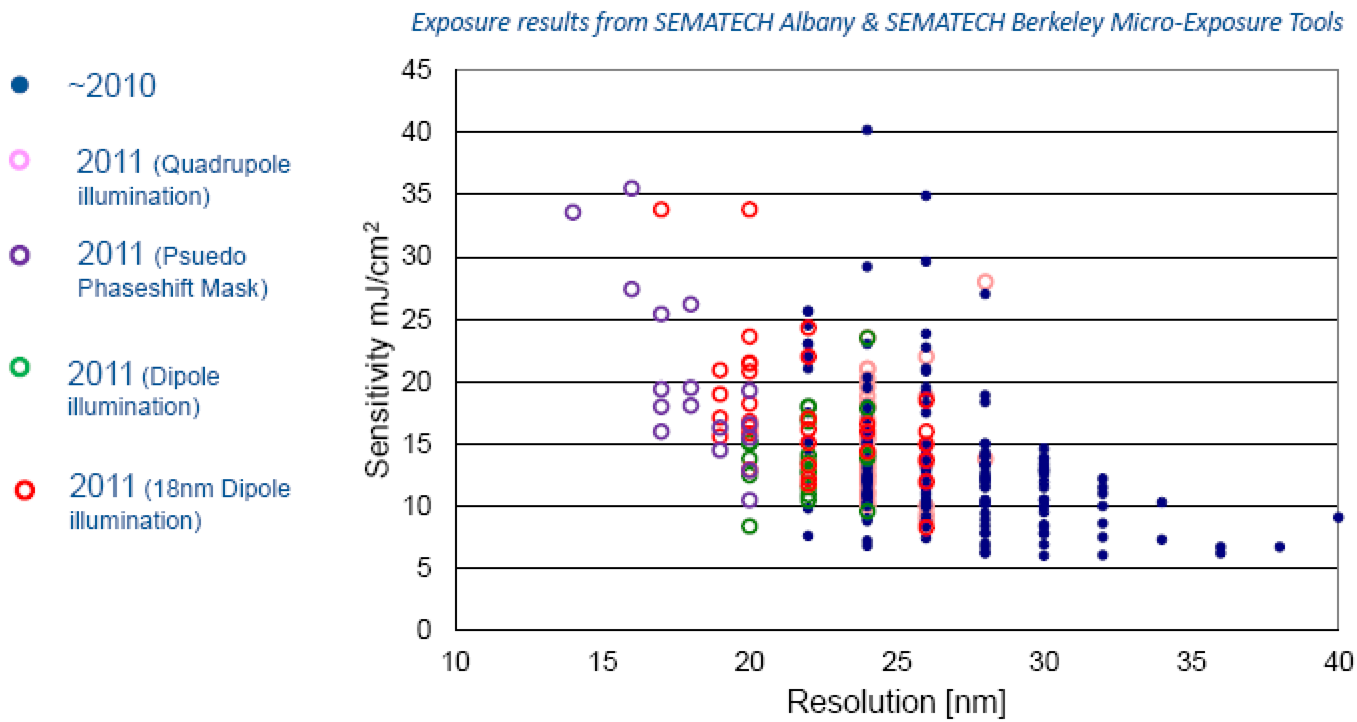
EUV Litho, Inc.

Source: S. Wurm, 2012 Semicon West

Resolution OK but sensitivity needs to improve by 2 to 3 x

EUV Resist Performance Status

Sensitivity vs. Resolution



- Resolution down to 15 nm has been demonstrated by using optimized illumination conditions.

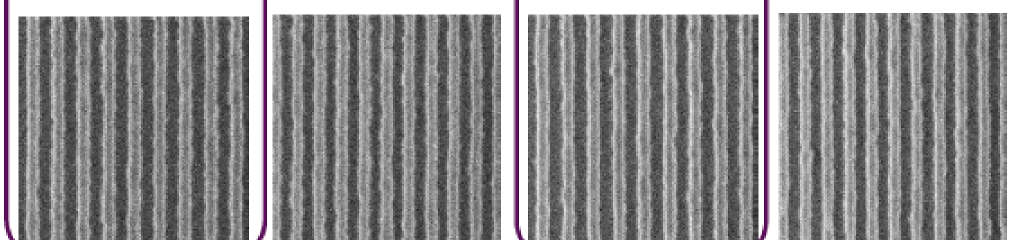
Source: S. Wurm, 2012 Semicon West

LER of ~3.2 nm for 25 nm L/S via Post Processing

APPLICATION OF FIRM RINSE EFFECT ON LER AND PROCESS WINDOW

	DI-water rinse		Firm rinse	
CD	L25P50	L22P44	L25P50	L22P44
Dose to size	13.2mJ/cm2	13.3mJ/cm2	14.5mJ/cm2	14.6mJ/cm2
3 sigma LER	3.5nm	3.9nm	3.2nm	3.5nm
Max Exp latitude	19.4%	4.8%	20%	5.7%
Max DOF	240nm	120nm	200nm	120nm

NXE :3100
Resist D @40nm
E2stack AL412@ 20nm



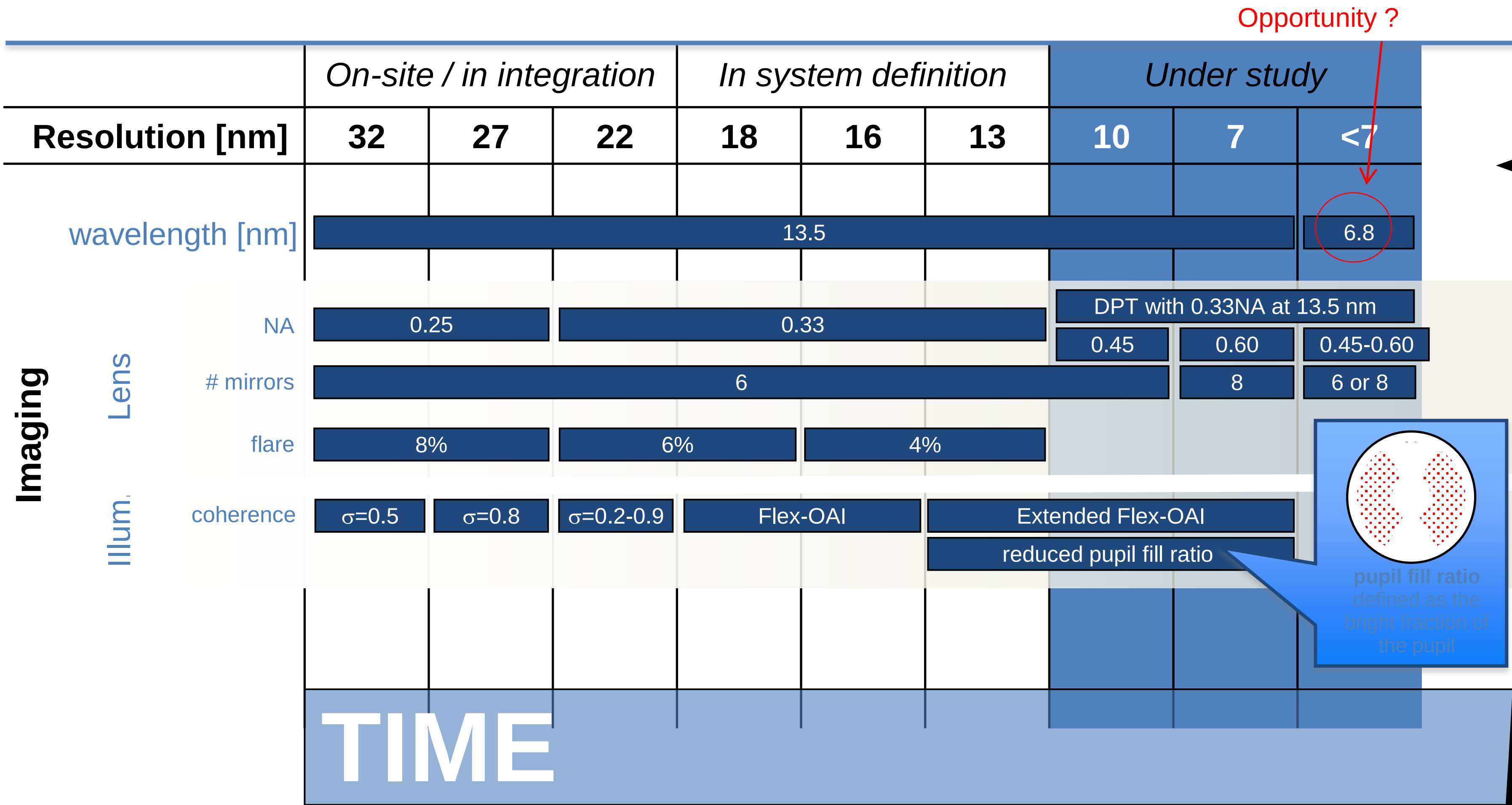
25nm LS performance is meeting the specification for sensitivity and latitudes and is very close to the LER target. Small improvement in latitude with Firm rinse but 9% reduction in LER.

EUVL Technology Status

EUV SCANNER STATUS

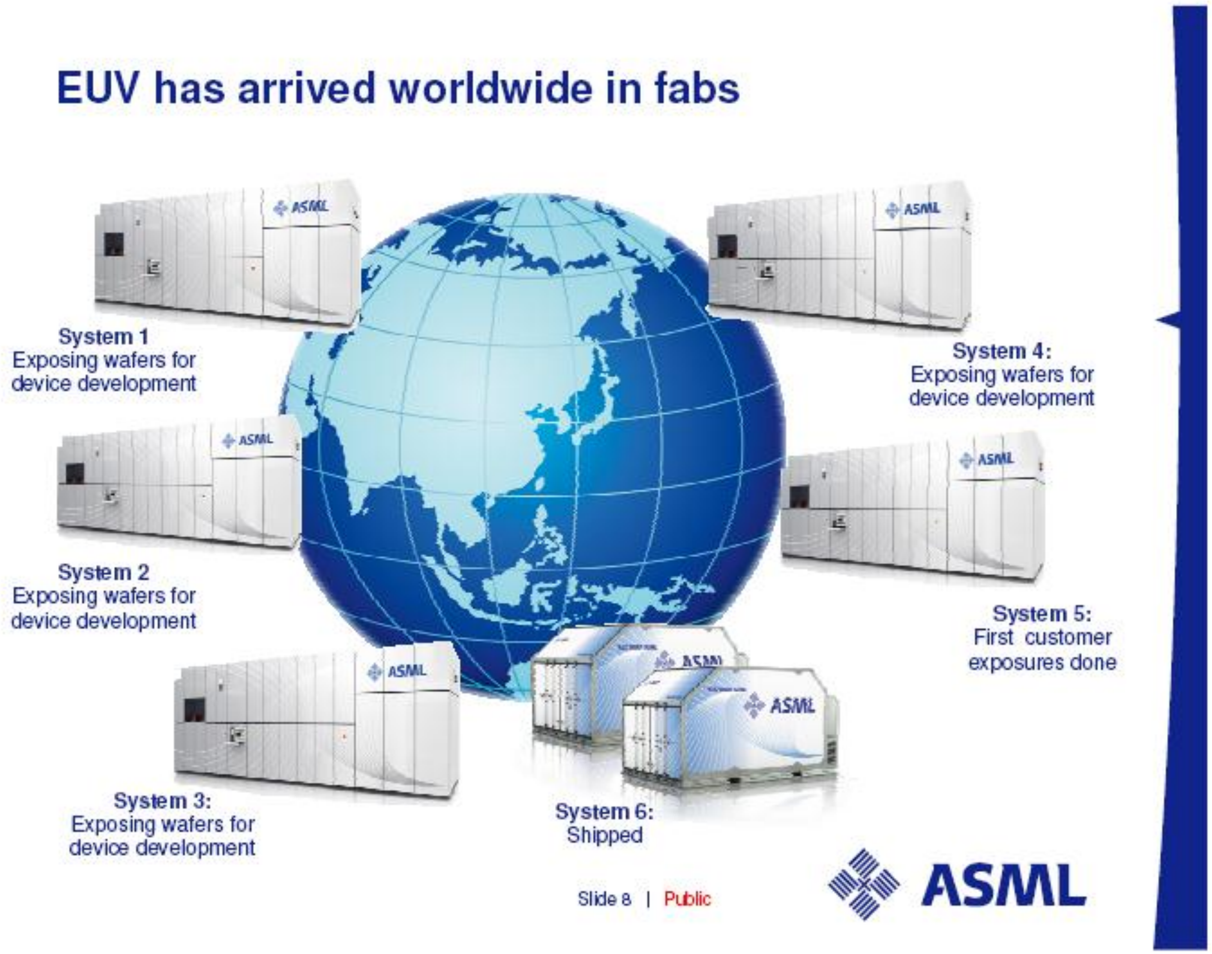
EUVL Scanner can be extended to < 7 nm resolution

first illumination optimization, then NA increase



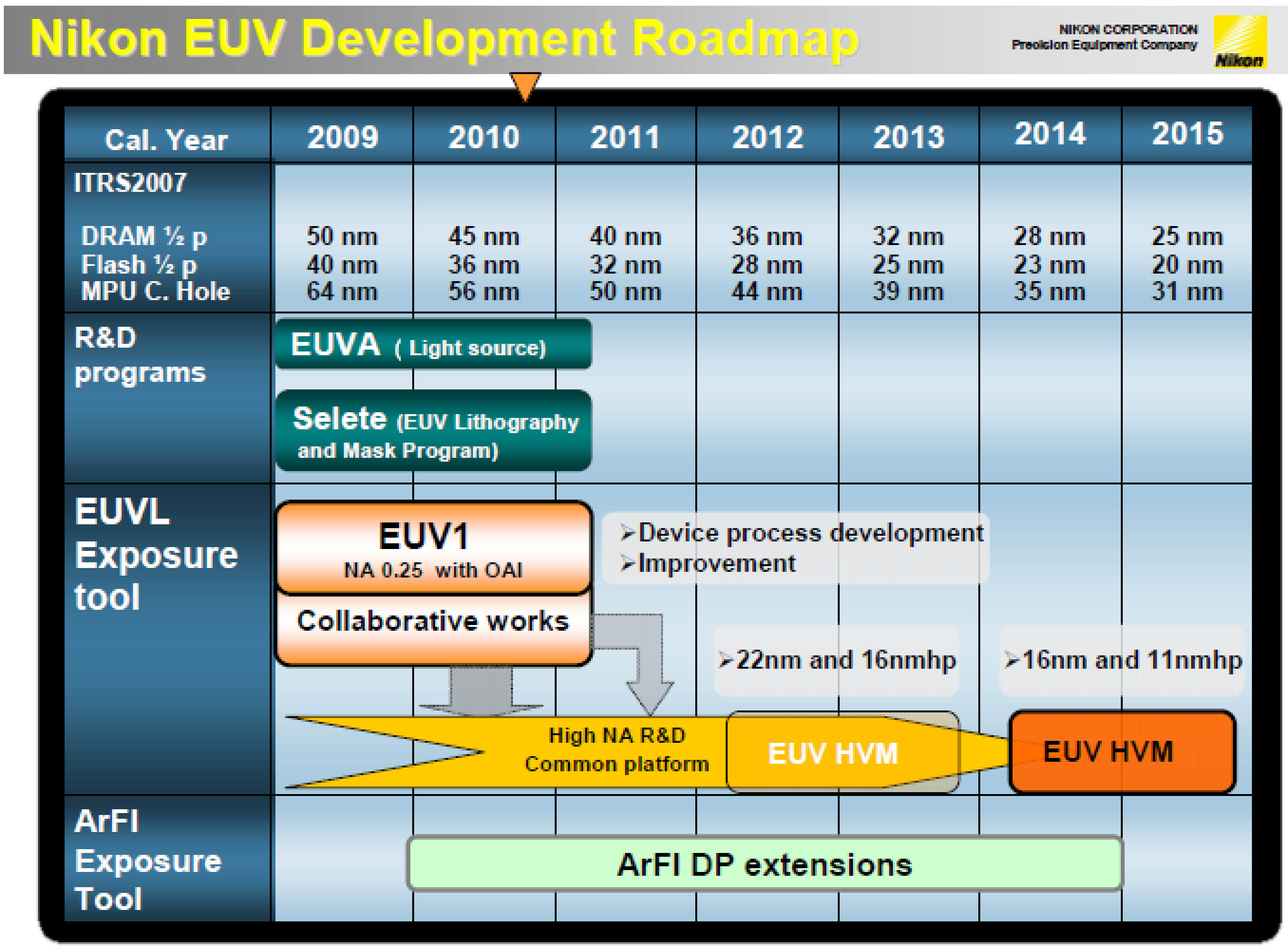
Source: V. Banine, 2012 Source Workshop

NXE 3100(β level EUVL Scanner) Six scanners Operating in Field



Courtesy: ASML, October, 2011

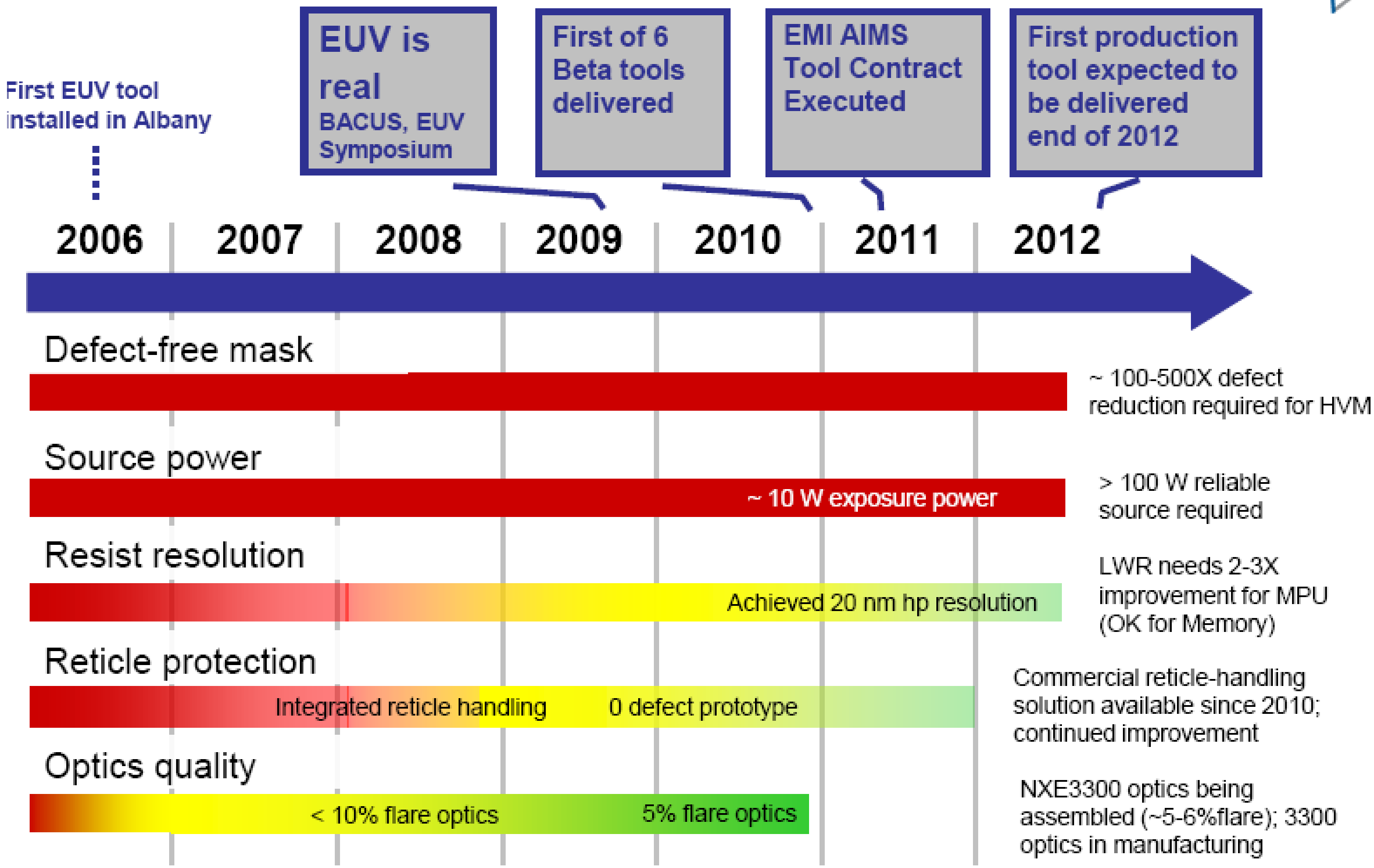
Nikon: In-house Learning for β Level and will Provide HVM Scanners Only



EUVL Technology Status

EUVL STATUS SUMMARY

EUV Infrastructure Readiness



Source: S. Wurm, 2012 Semicon West

Optical Lithography Challenges (ITRS 2011)

- **Near Term Challenges (2011-18)**
  - EUV source power to meet throughput requirement
  - Defect "free" EUV masks availability mask infrastructure availability
  - EUV mask in fab handling, storage, and requalification.
  - Resist at 16nm and below that can meet sensitivity, resolution, LER requirements
  - Retooling requirements for 450mm transition

Optical Lithography Challenges (ITRS 2011)

- **Long terms (2019-2025)**
  - Higher source power
  - Increase in NA, chief ray angle change on EUV
  - Mask material and thickness optimization
  - Infrastructure for 6.Xnm Lithography or multiple patterning for EUVL 13.5nm

EUV Litho, Inc.

Outline

- Introduction to EUV Lithography
- Technical Status and Challenges
- Summary

Summary

- Today EUVL is in Process Development phase
- Six β level scanners (NXE 3100) are in field
- HVM Scanners (NXE 3300) are to be delivered starting Q4 2012
- EUVL is expected to be adopted for HVM by at least some leading edge chipmakers by 2014!
- **Continued R&D needed to provide innovative solutions to current EUVL technical challenges and prepare the EUVL technology to support pattering until the end of Moore's Law**

EUV LITHO, INC.